Reliability and Ruggedness of Commercial SiC Power MOSFETs

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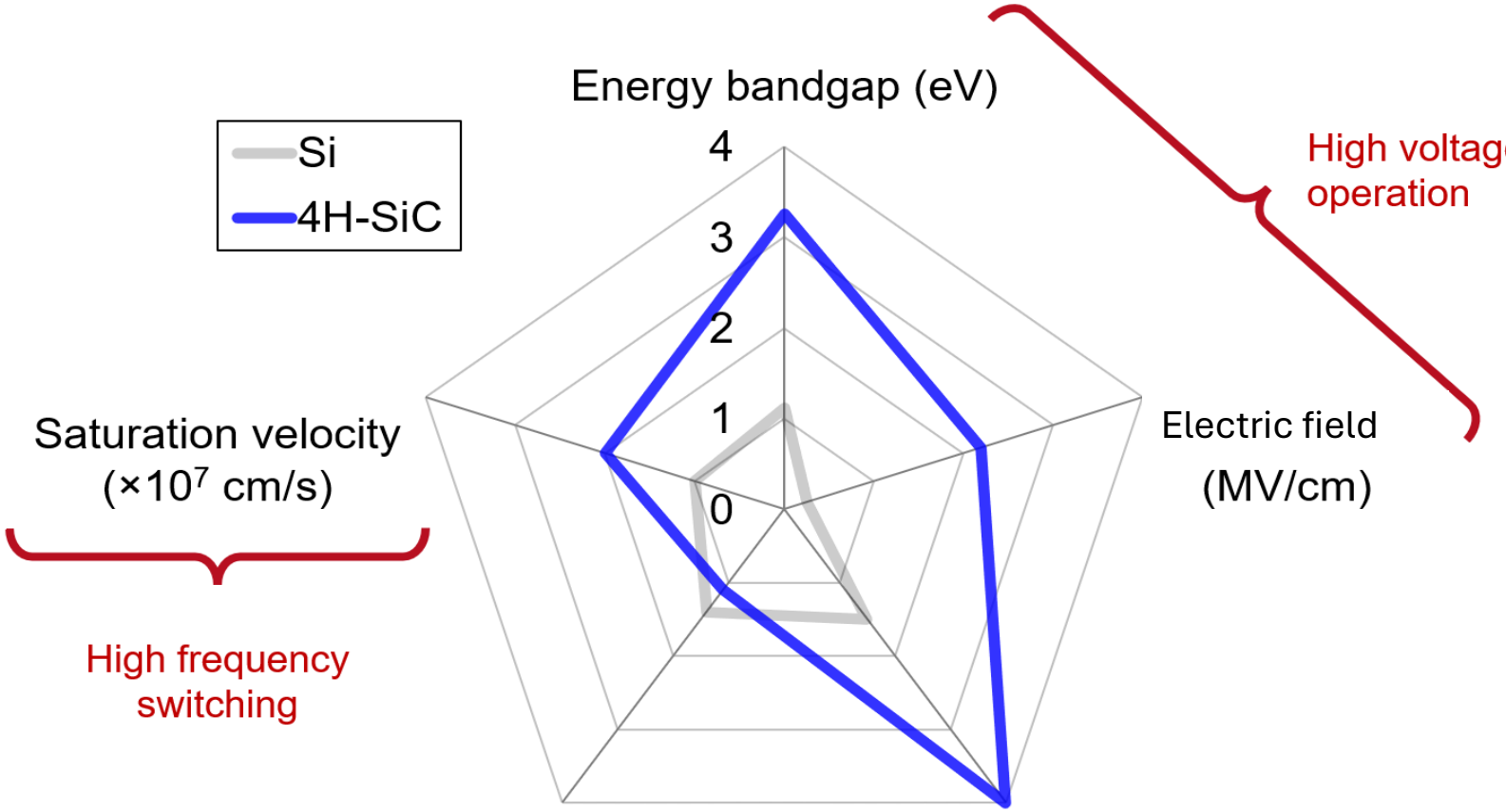
Advantages of 4H-SiC Material

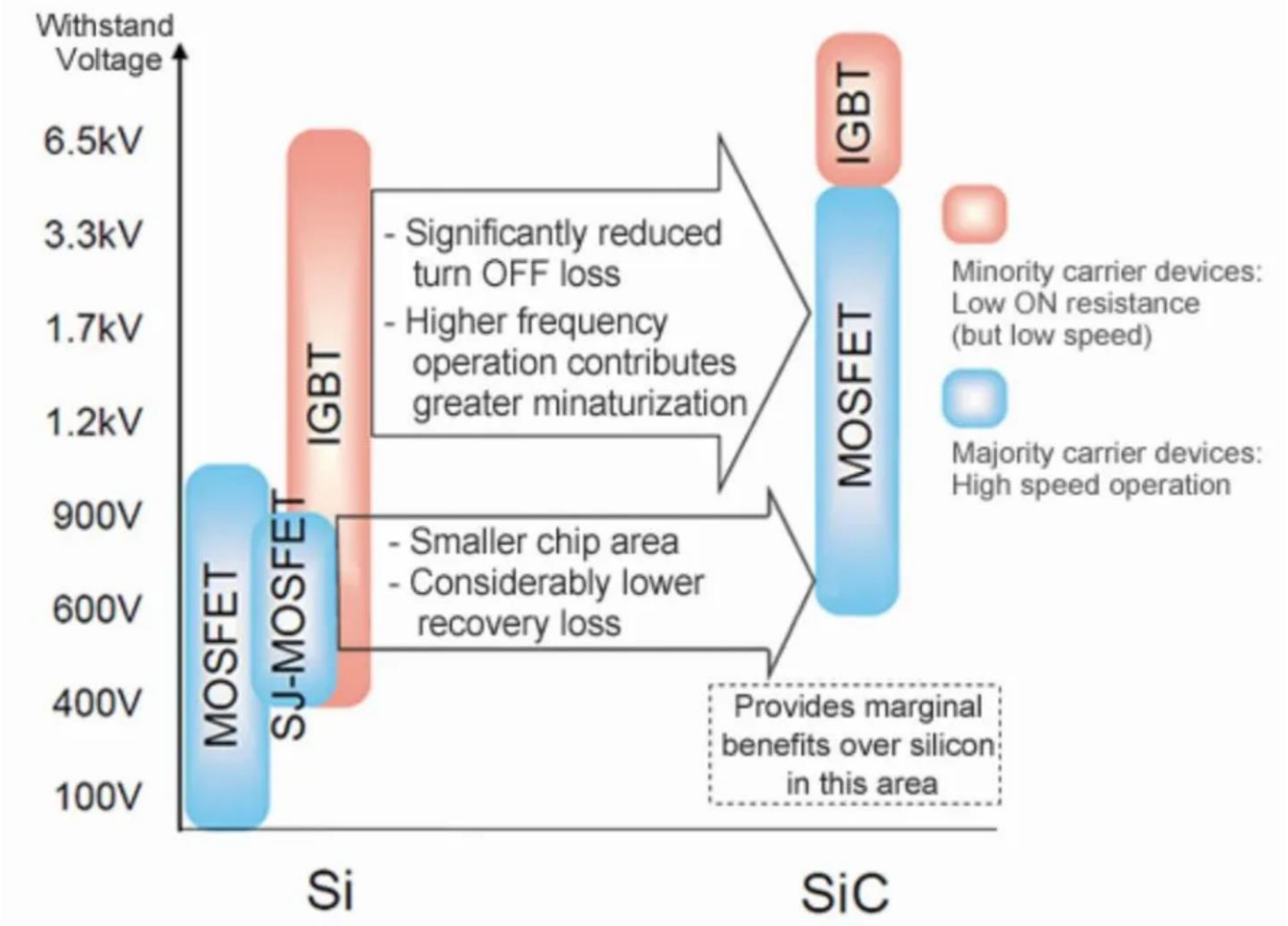


High voltage operation

High frequency switching

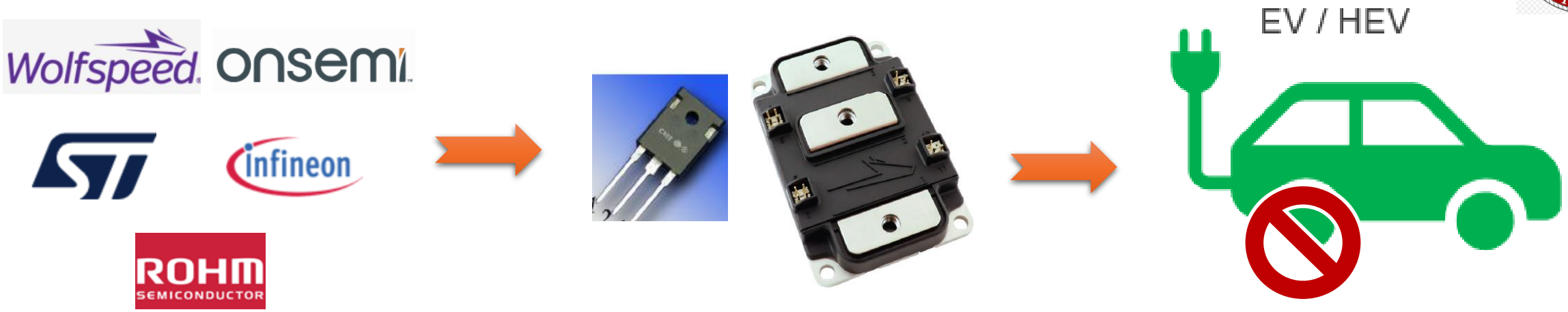
High temperature applications

Advantages of 4H-SiC Power MOSFETs



Demystifying SiC MOSFETs challenges - Power Electronics News

Motivation



- 2%-3% failure of SiC MOSFETs in EV inverters in the field.

1. Gate Oxide Early Failure
2. Weak Short Circuit Ruggedness

} Reliability Issues

- Develop effective screening approach to reduce the probability of extrinsic failures.
- Develop effective screening approach to identify SiC MOSFETs with shorter SCWT.

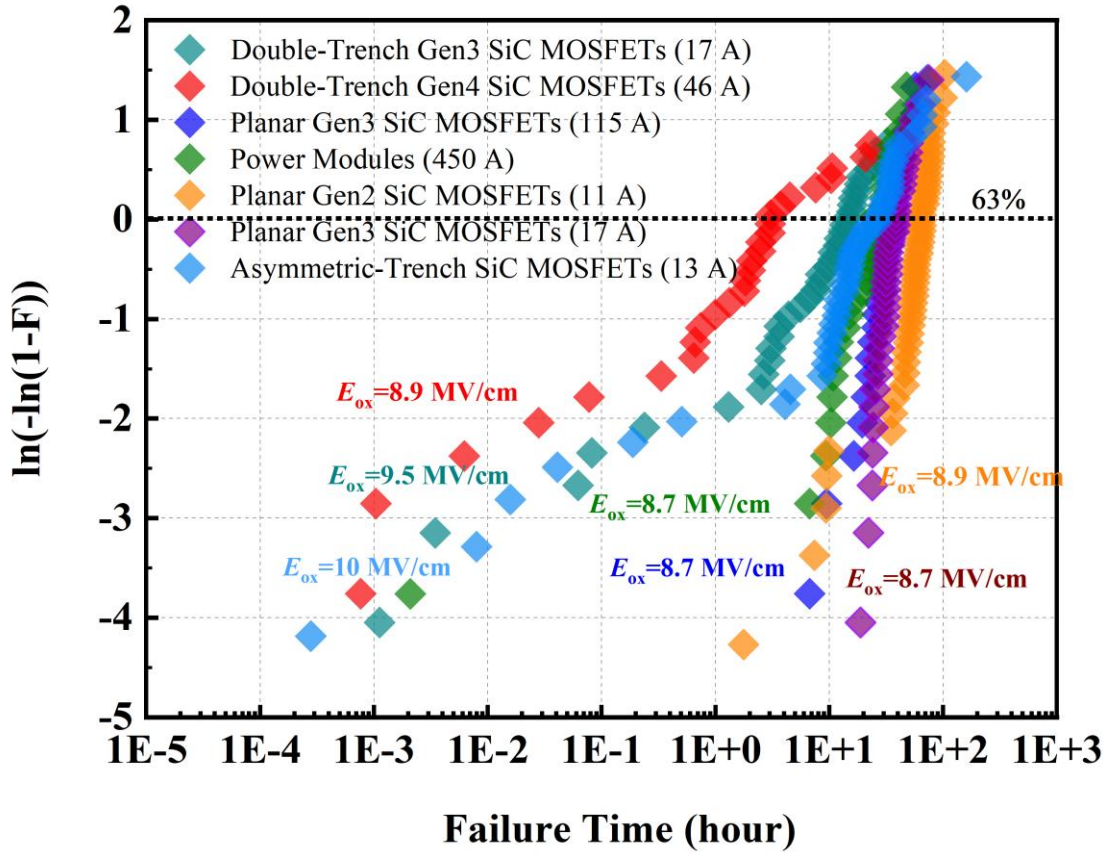
Topic

1. Analysis and Optimization of Screening Techniques

2. A Non-destructive Short Circuit Withstand Time Screening Methodology

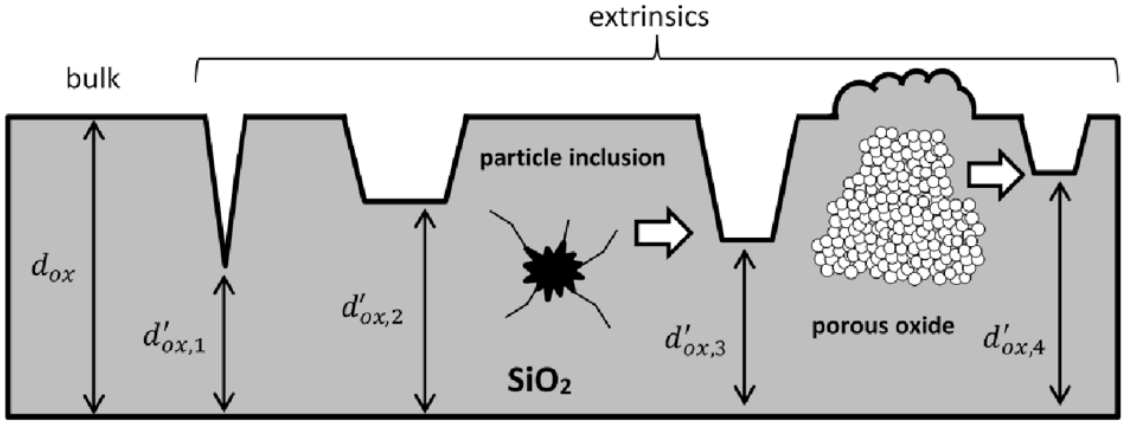
Major Challenge of SiC MOSFETs in EVs

- **Gate oxide failure: Higher risk for early GOX breakdown**
- **EV requirement: Gate oxide lifetime >> 20 years at 150℃**



Origin of Early Failures —— Oxide Thinning Model

Substrate defects
particles
process variations



$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{V_{ox}}{t_{ox} - \Delta t_{ox}} = \frac{V_{ox}}{t_{eff}}.$$

[1] Aichinger et al. 2020. IRPS

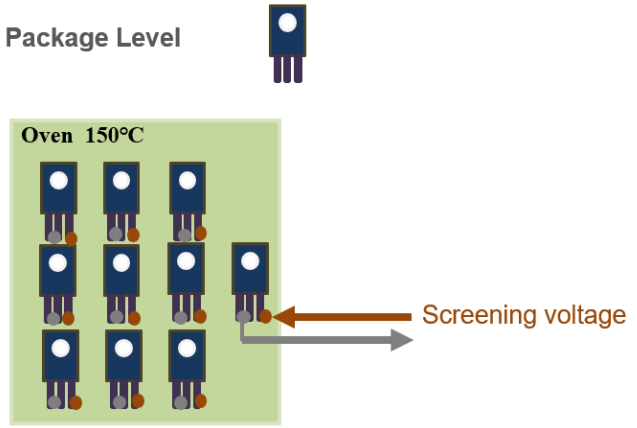
Extrinsic defect → Effective oxide thickness ↓ → Locally electric field ↑ → Early breakdown

- **The individual devices with large extrinsic defect density have a high failure probability.**

Purpose

Conventional Screening Technology → **Package-Level Burn-in** →

Long Stress Time

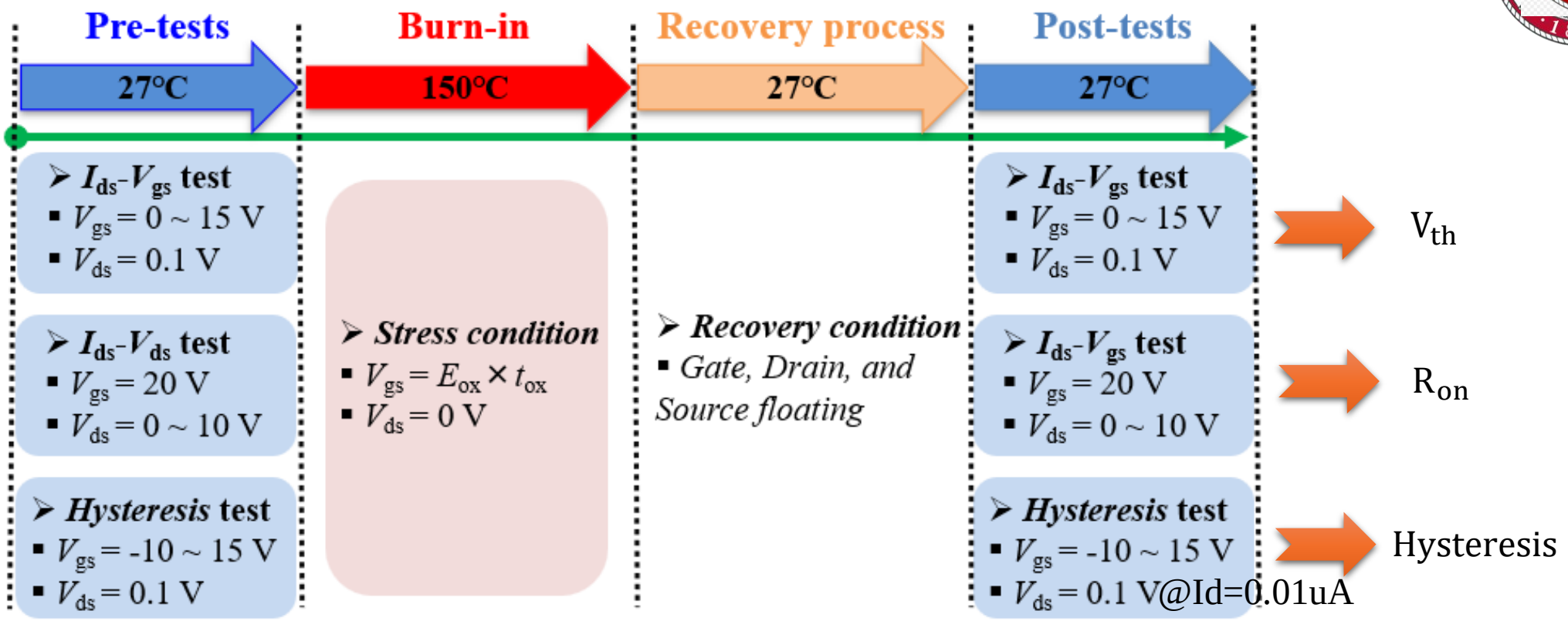


- **Function of burn-in**
  - Devices with extrinsic fail + Devices without critical extrinsic pass
- **Disadvantage of burn-in**
  - Time-consuming
  - Large V_{th} shift
- **Objective**
  - Not degrade device performance (Threshold voltage, On-resistance, Interface defect, and Oxide intrinsic lifetime)
  - Improve efficiency (Increase voltage during Burn-in)

Analysis and Optimization of Screening Techniques

- Introduction
- Impact of Burn-in Techniques on SiC MOSFETs
  - Effects of Burn-in on the Performance of SiC MOSFETs
  - Effects of Burn-in on the Interface States of SiC MOSFETs
- Optimized Burn-in Techniques
  - Burn-in Technique based on the Critical Stress Time
  - Pulse-mode Burn-in Technique

Test Procedure



$$\Delta V_{th} = V_{th-post} - V_{th-pre}$$

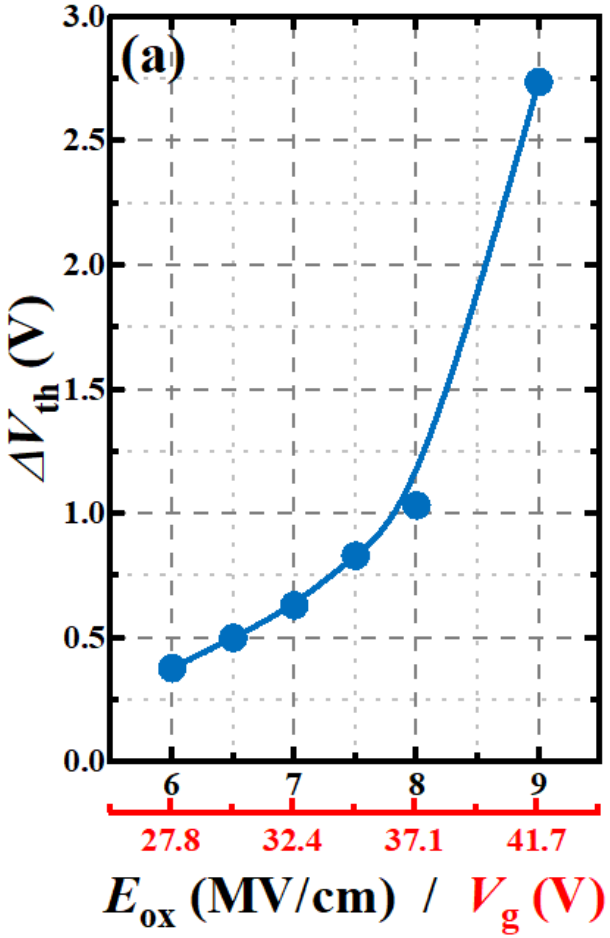
$$\Delta R_{on} = R_{on-post} - R_{on-pre}$$

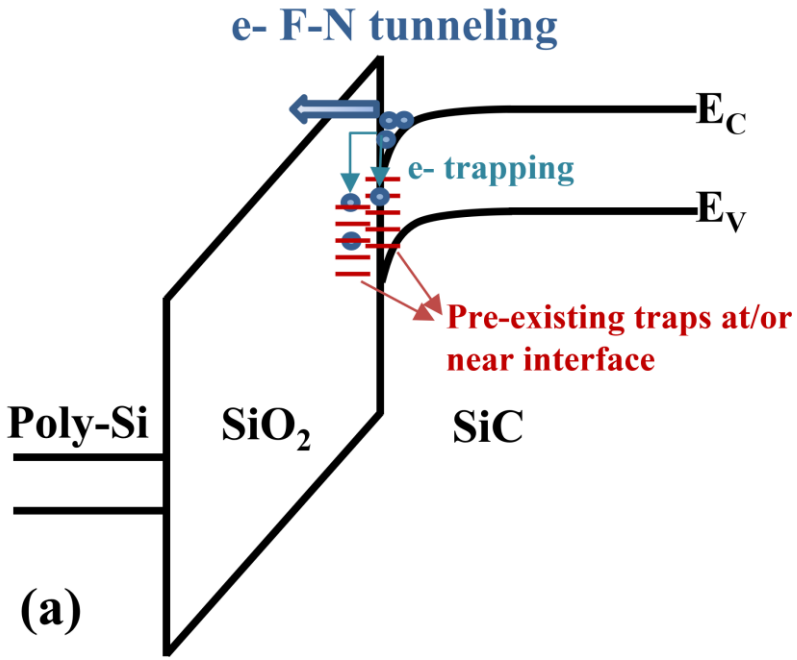
$$\Delta Hysteresis = Hysteresis_{post} - Hysteresis_{pre}$$

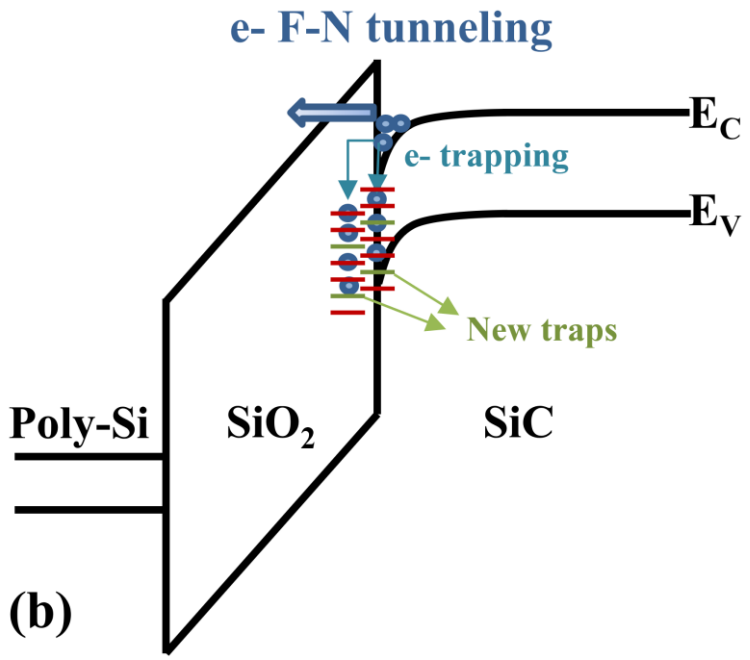
Degradation Rate (DR) =Δ / initial value

Large Threshold Voltage Shift

Burn-in stress time is 10 hours



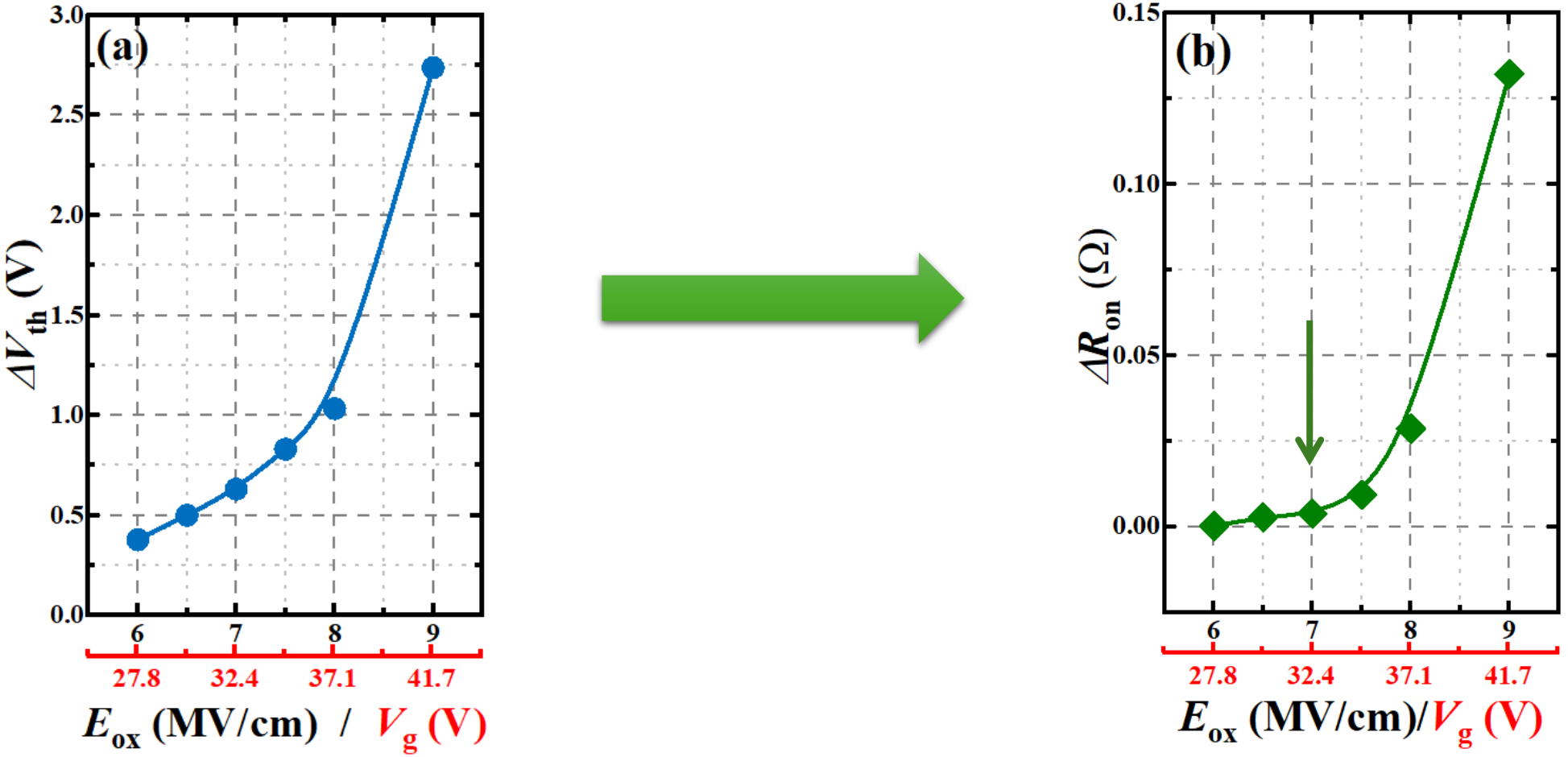




The large V_{th} shift

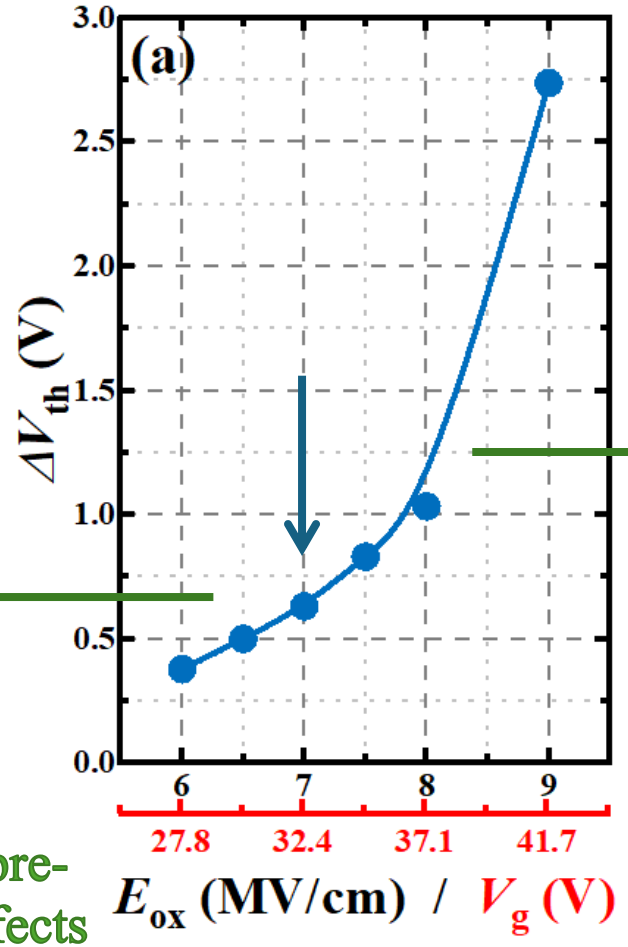
- A large number of electrons being injected and subsequently trapped by pre-existing defects at or near the interface.
- An increase in the D_{it} during the burn-in process

On-resistance Increase



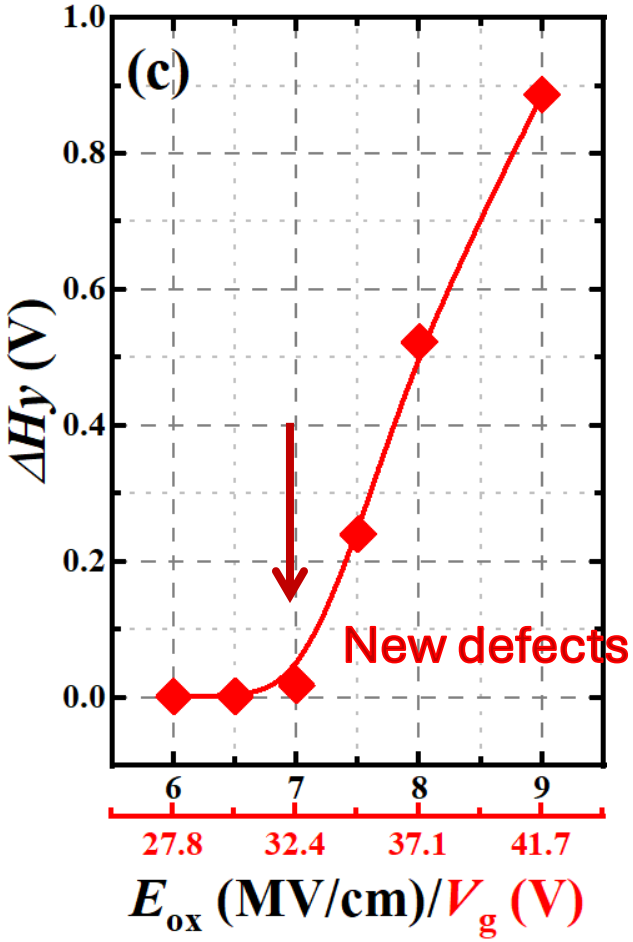
- Electron trapping results in positive V_{th} shift and a reduction in carrier mobility, thereby increasing the on-resistance.

Hysteresis Increase



Electrons trapped in pre-existing defects

Defect generation exacerbate the V_{th} shift



New defects generate

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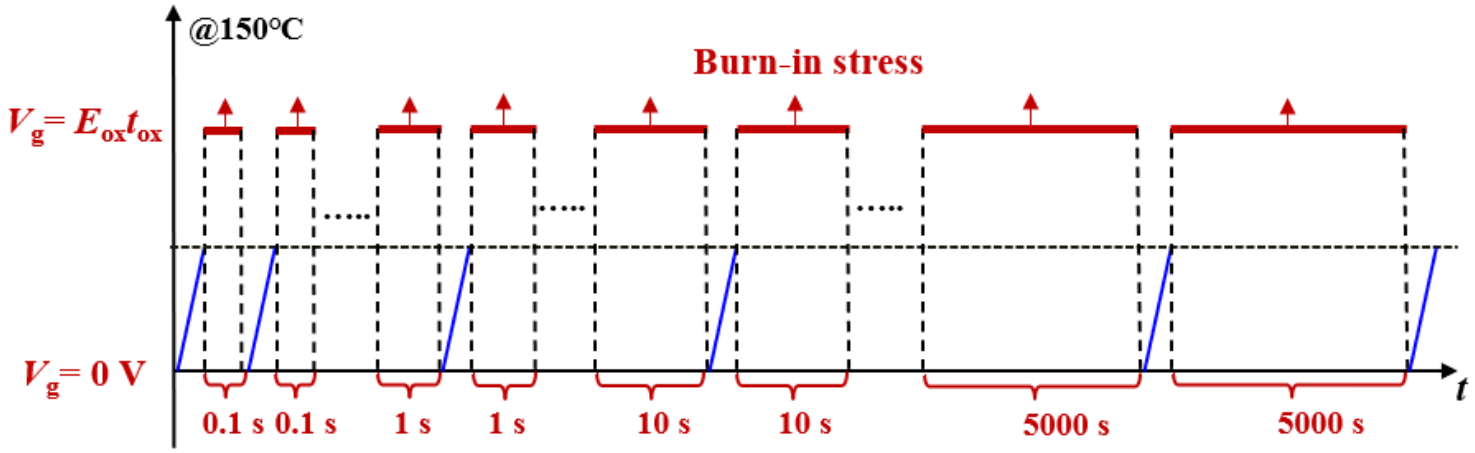
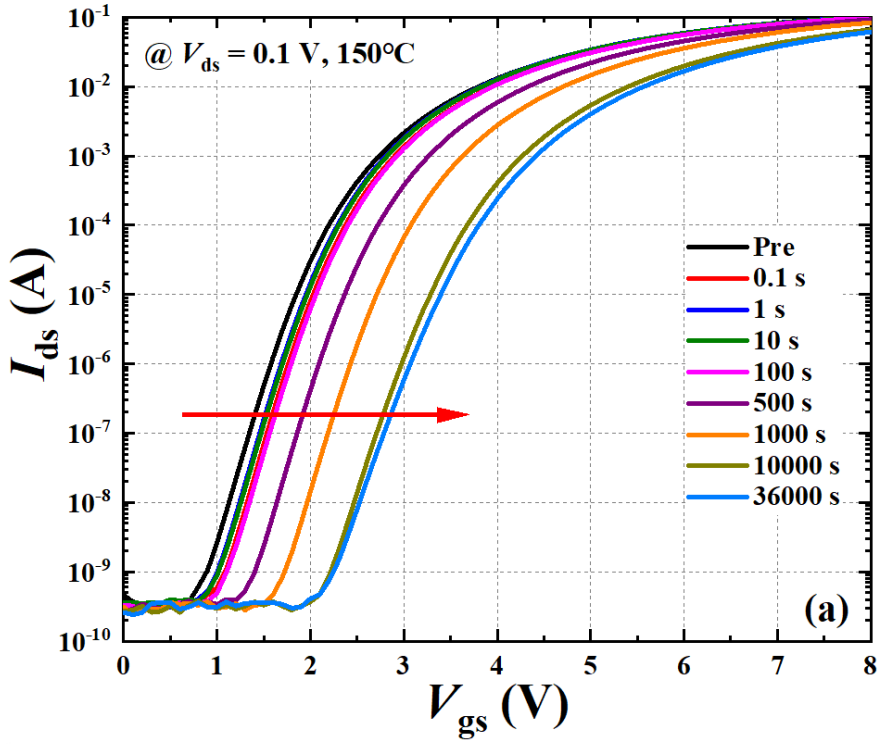
  - Burn-in Technique based on the Critical Stress Time
  - Pulse-mode Burn-in Technique

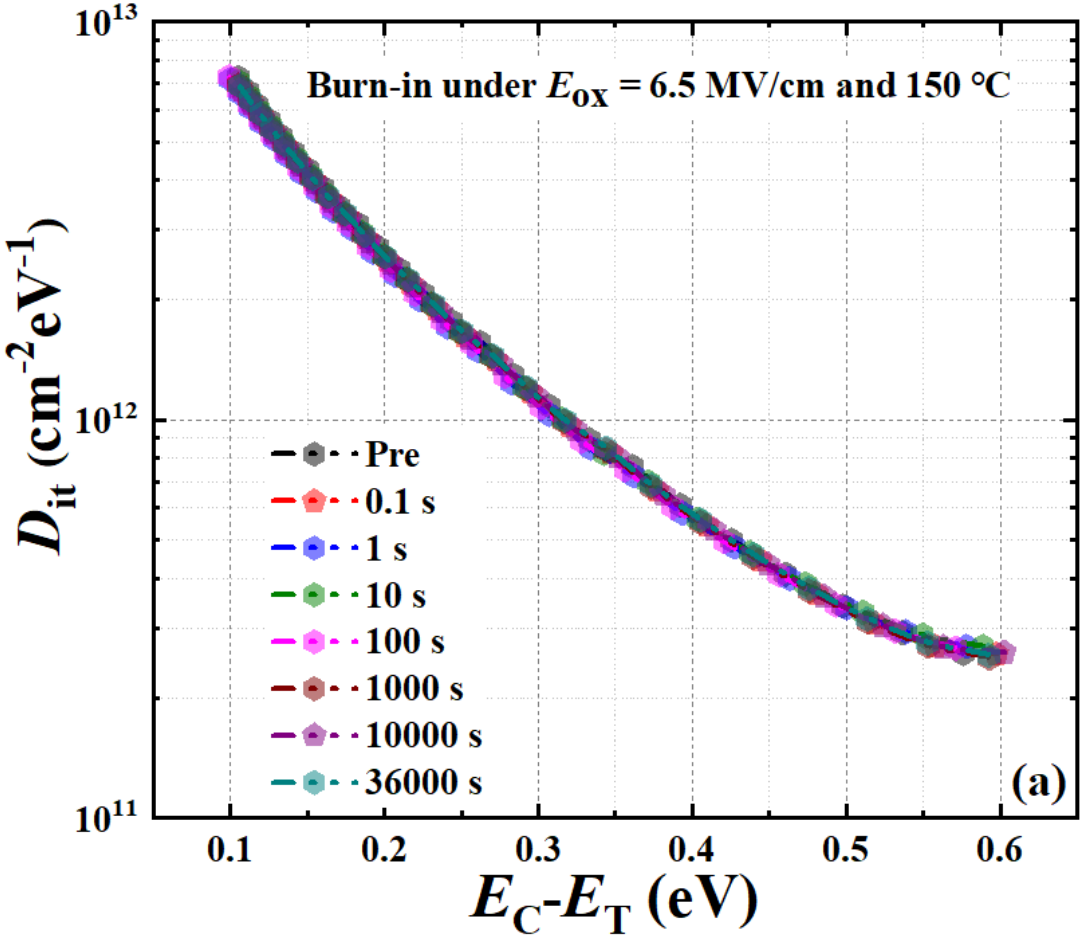
Test Procedure for Transfer Curves

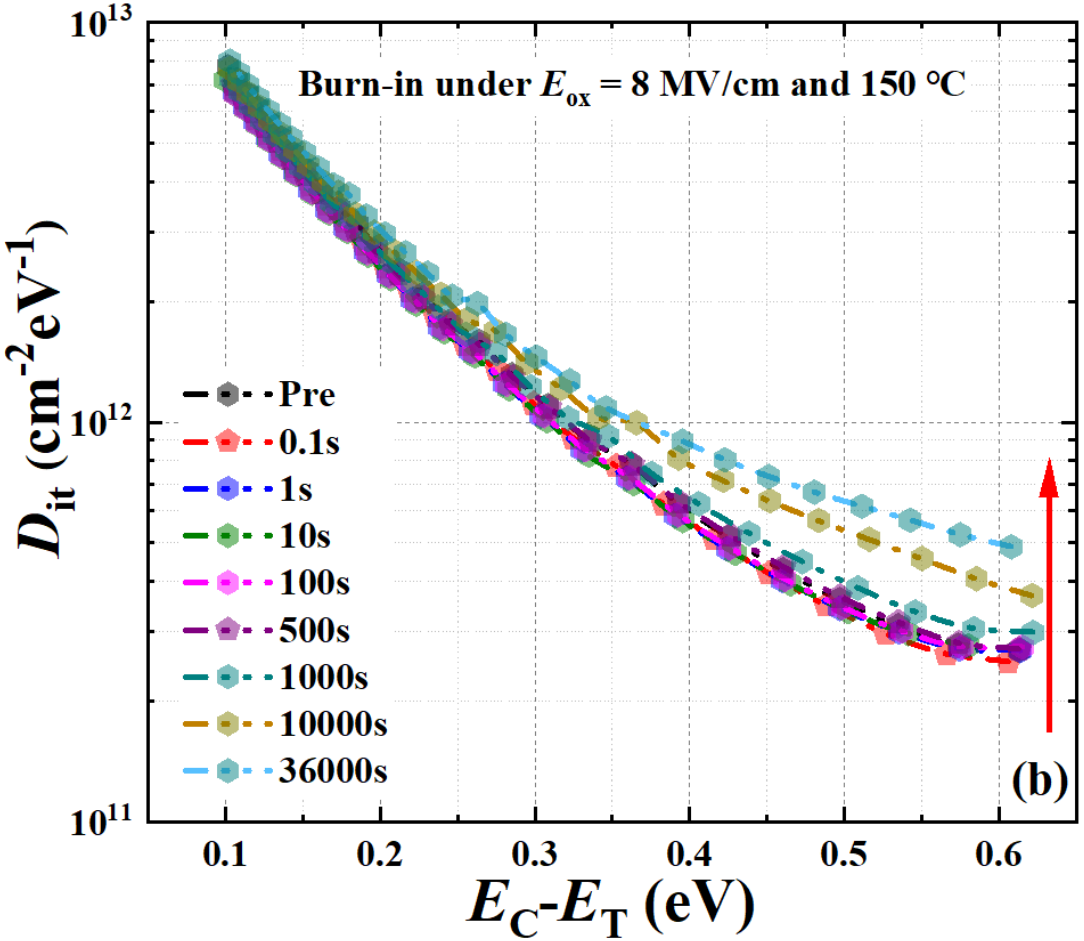




Transfer curve in the subthreshold region → Interface state density (D_{it})

Interface Defects Generation Under High-E_{ox} Stress





❖ No degradation on interface state.

❖ Interface Defects Generation.

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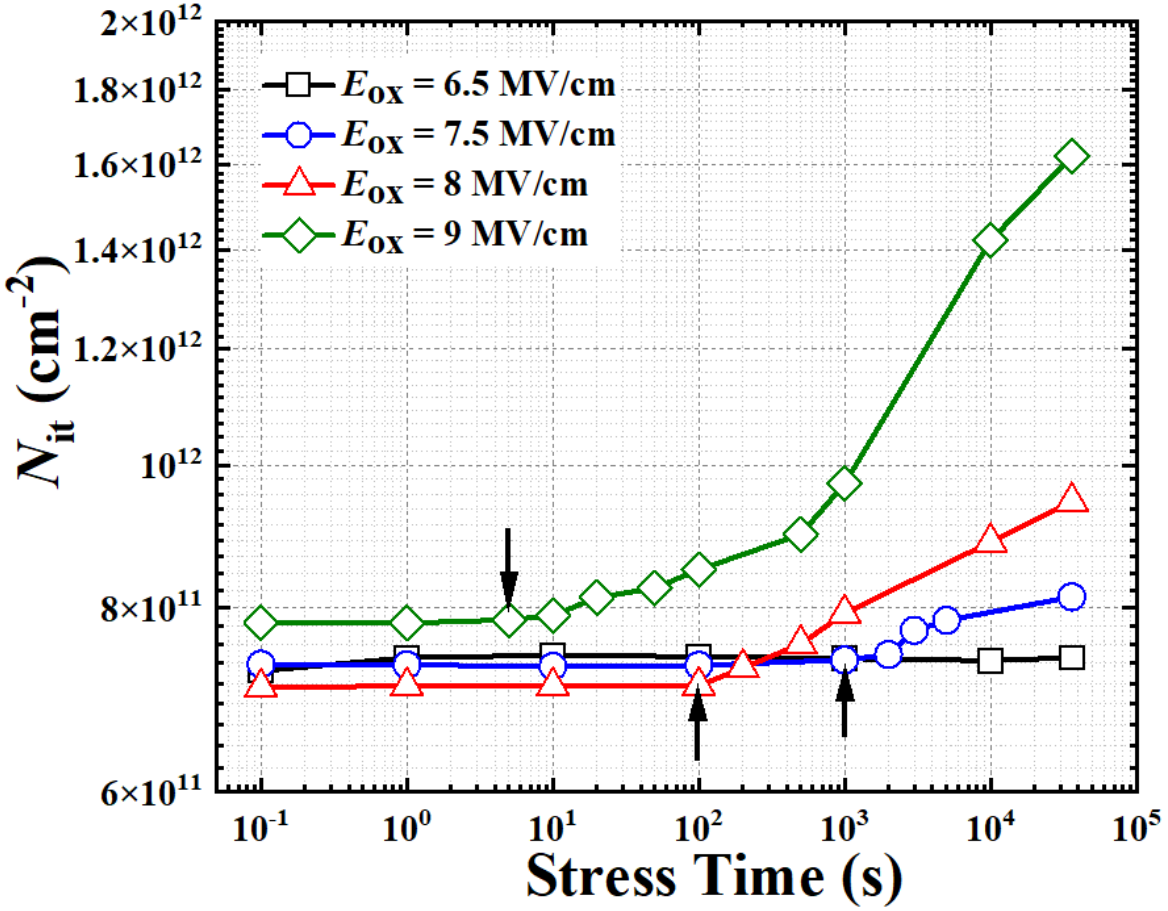
Identify Critical Stress Time



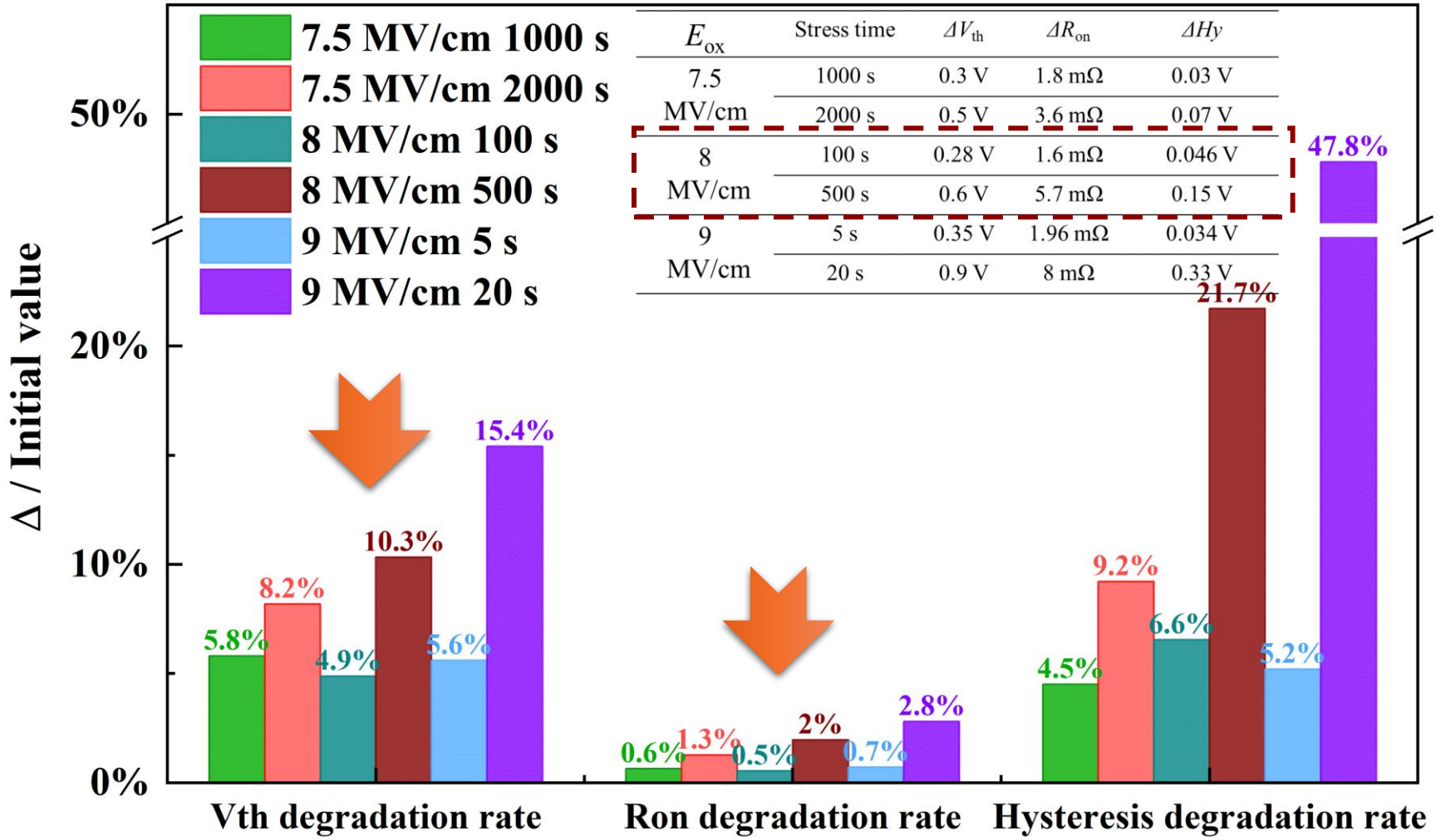
Number of traps

$$N_{it} = \int_{E_{cs}-E_{T0}}^{E_{cs}-E_{T1}} D_{it} dE_T$$

E_{ox} at 150℃	Critical time
7.5 MV/cm	< 1000 s
8 MV/cm	< 100 s
9 MV/cm	< 5 s

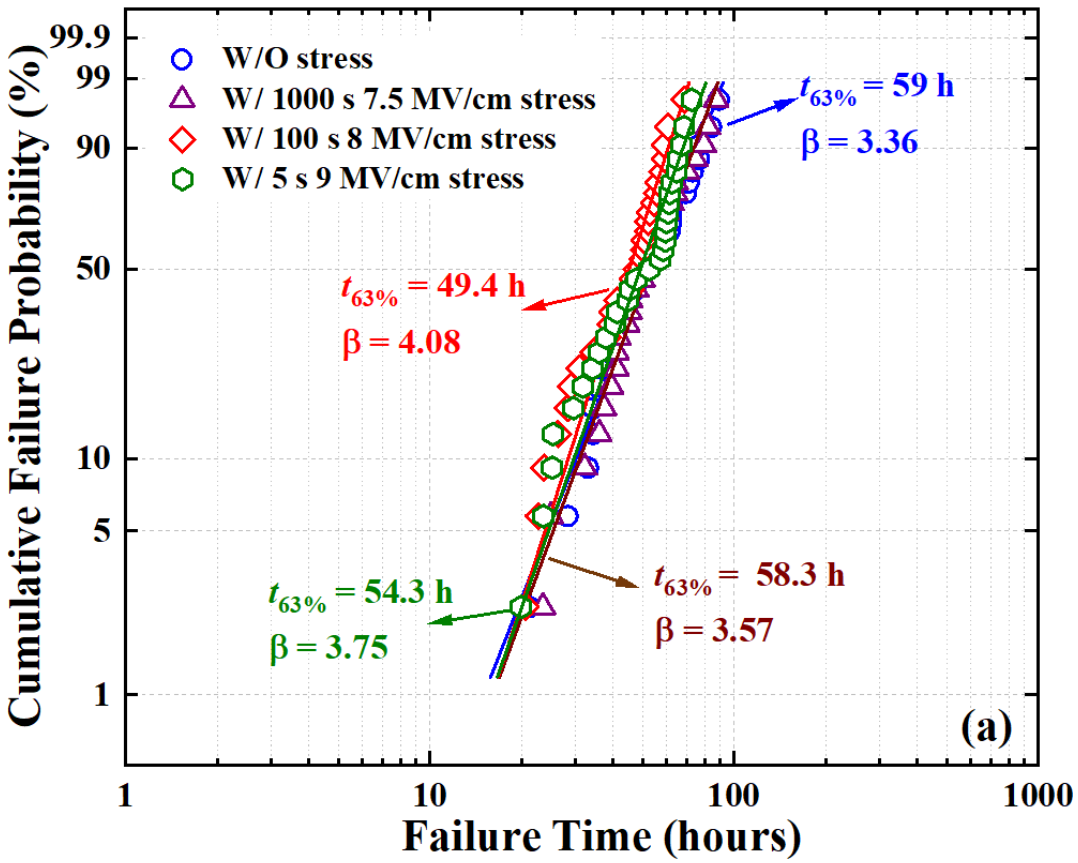
❖ The Recommended Burn-in Conditions can avoid the increase of D_{it} during the burn-in process.

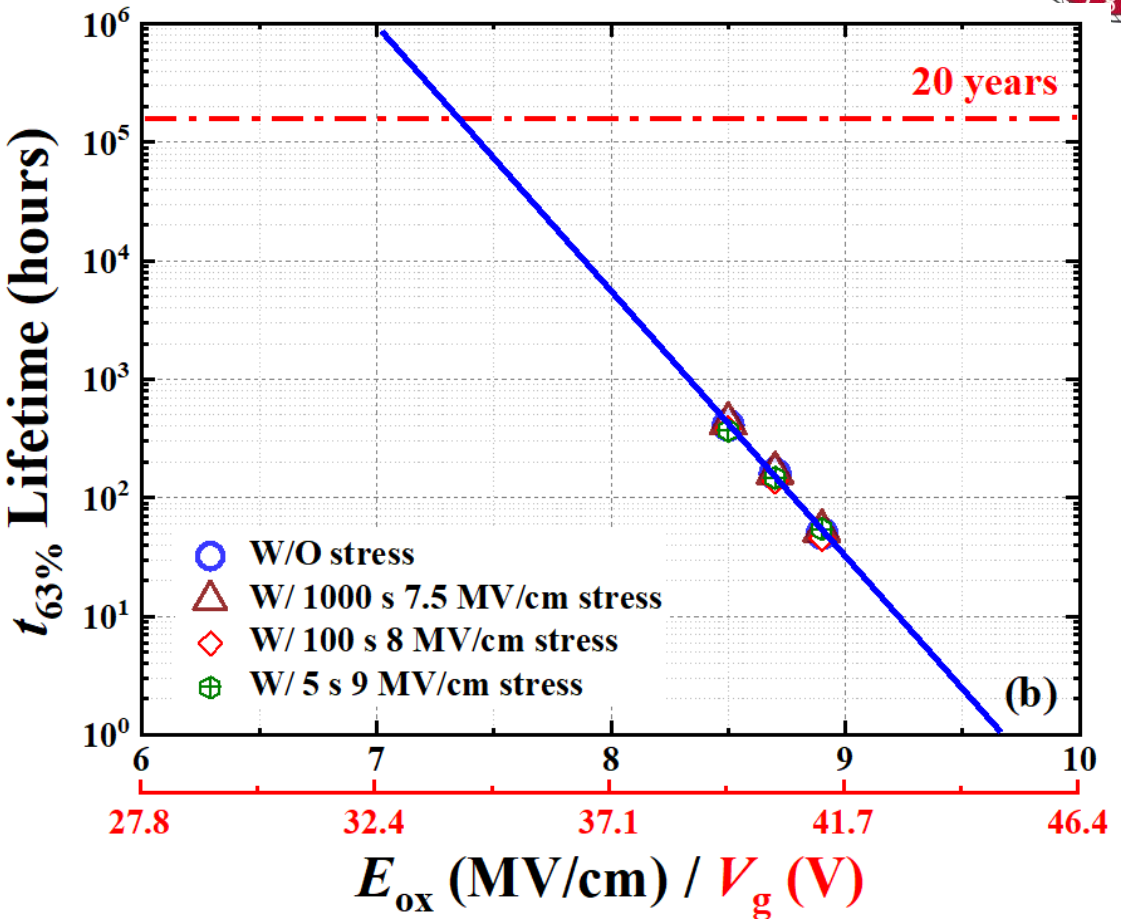
Effectiveness of Burn-in based on the Critical Stress Time



E_{ox}	Stress time	ΔV_{th}	ΔR_{on}	ΔHy
7.5 MV/cm	1000 s	0.3 V	1.8 mΩ	0.03 V
	2000 s	0.5 V	3.6 mΩ	0.07 V
8 MV/cm	100 s	0.28 V	1.6 mΩ	0.046 V
	500 s	0.6 V	5.7 mΩ	0.15 V
9 MV/cm	5 s	0.35 V	1.96 mΩ	0.034 V
	20 s	0.9 V	8 mΩ	0.33 V

No Degradation in Oxide Intrinsic Lifetime





- Recommended burn-in technique does not have an obvious negative impact on the gate oxide intrinsic lifetime of the SiC MOSFETs.

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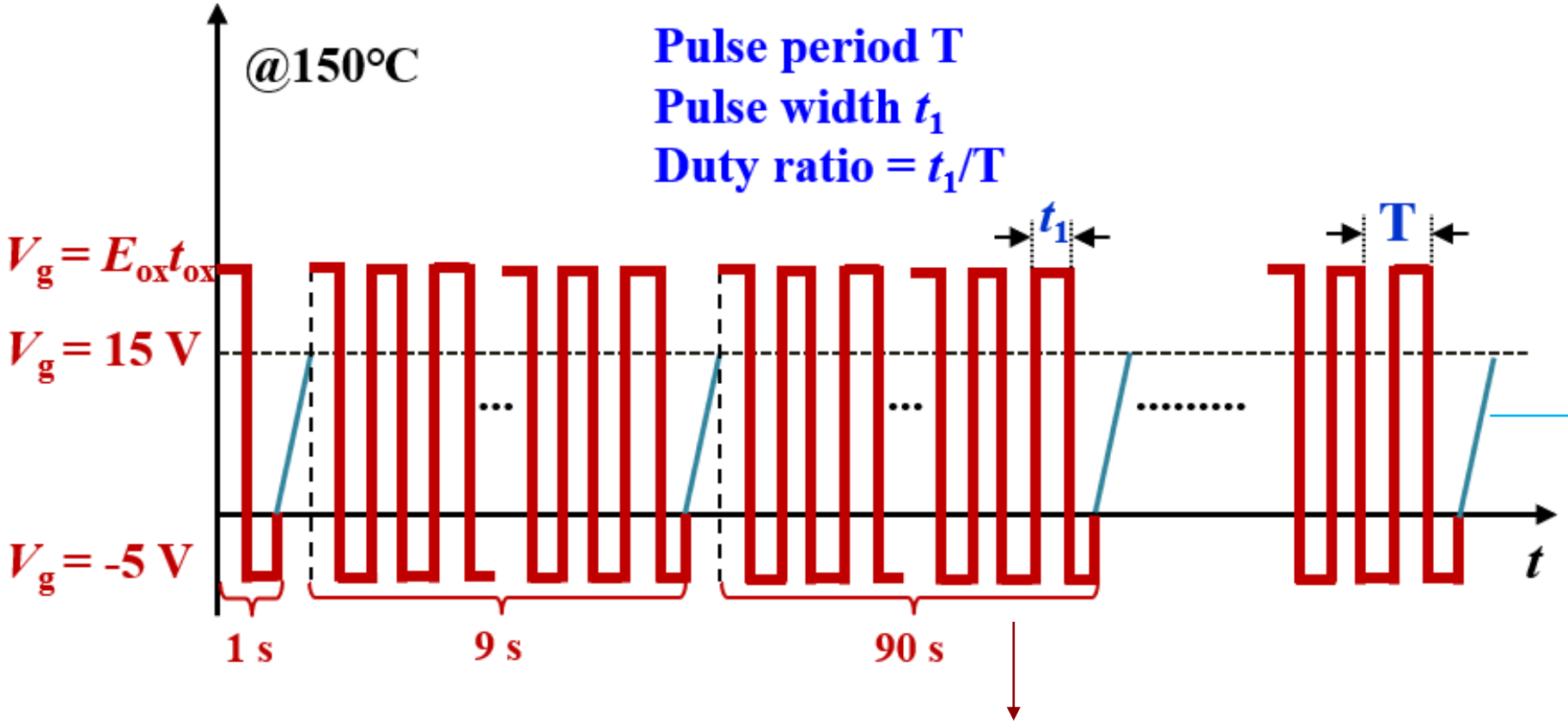
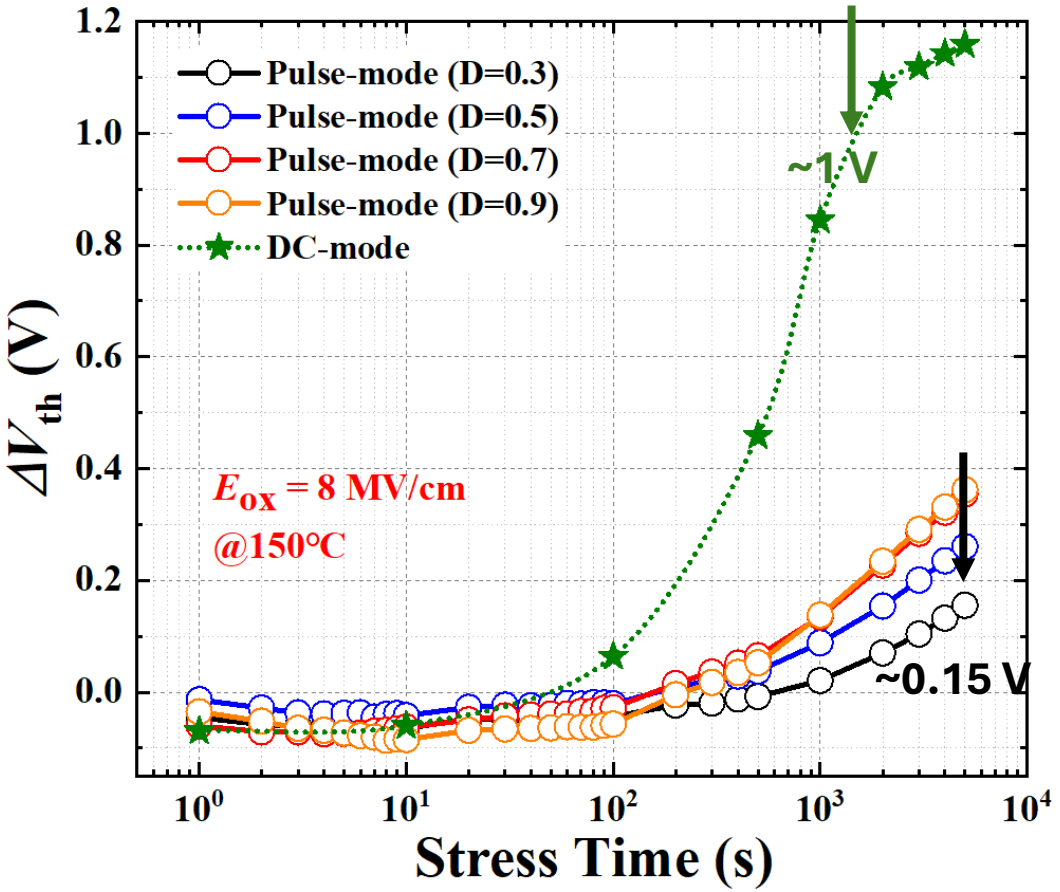
Pulse-mode Burn-in Setup

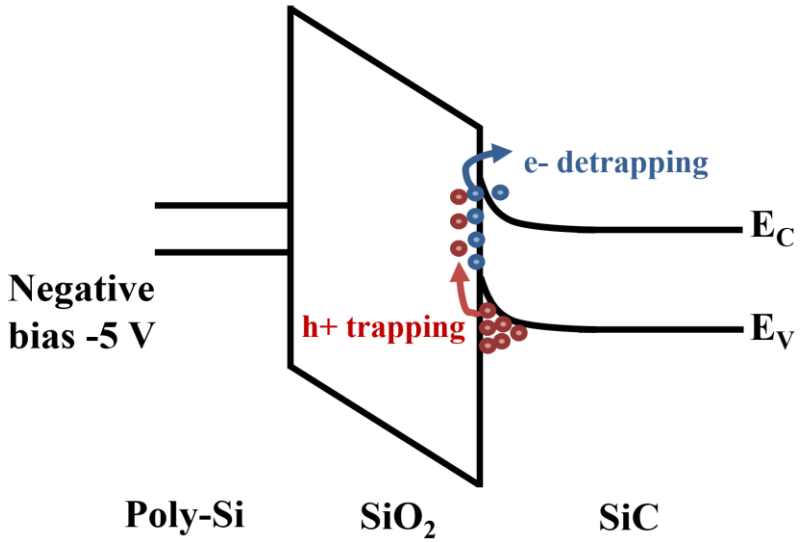


Transfer Test
V_{gs}=0~15V

Burn-in Stress
V_g= -5 / $E_{ox}t_{ox}$

Applying a Negative Voltage Facilitates Recovery of V_{th}





- The holes accumulated in the valence band are captured by oxide traps.
- The captured electrons under positive voltage tunnel back into the conduction band.

Positive Stress Time= Stress Time × Duty Ratio

Effect of Burn-in

E_{ox} (MV/cm)	Burn-in mode	Time (s)	ΔV_{th} (%)	ΔR_{on} (%)	ΔHy (%)	$t_{63\%}$ (h)
7.5	DC	1000	5.8	0.6	4.5	58.3
		2000	8.2	1.3	9.2	53.6
	Pulse	4000	0.5	1.3	3.8	52.7
8.0	DC	100	4.9	0.5	6.6	49.4
		500	10.3	2	21.7	47.3
	Pulse	1000	0.6	0.05	0.7	45.0
9.0	DC	5	5.6	0.7	5.2	54.3
		20	15.4	2.8	47.8	45.3
	Pulse	40	0.7	0.08	7.2	67.5

- The pulse-mode burn-in technique allows the device to be subjected to positive gate stress for a longer period of time while maintaining the non-degradation of the characteristics.

Conclusions and Outlook

- **Aggressive Burn-in Effects on Gate Oxide**: Aggressive burn-in treatments lead to electron accumulation in the gate oxide under positive gate stress and increase interface state defects at the SiC/SiO_2 interface.
- **Critical Stress Time**: For different screening electric fields, setting appropriate critical stress times and stopping stress before excessive charge injection into SiO_2 can prevent increased interface state defects.
- **Pulse-Model Burn-in**: Using pulse-model burn-in minimizes electron trapping due to positive gate stress, reducing positive threshold voltage shift. This allows SiC MOSFETs to undergo extended screening without significant performance degradation

- **Future Work:** Select a large batch of samples to validate the screening efficiency

Topic

1. Analysis and Optimization of Screening Techniques

2. A Non-destructive Short Circuit Withstand Time Screening Methodology

Outline

- **Background and Motivation**
  - Short Circuit Failure Basic
  - SiC MOSFET vs Si IGBT Short Circuit Withstand Time
  - SCWT Variation in Commercial SiC 1.2kV Planar Devices
- **Experiment Procedure and Samples**
  - Short Circuit Test Setup
  - Device Details
- **Novel Short Circuit Screening Methodology**
- **Summary**

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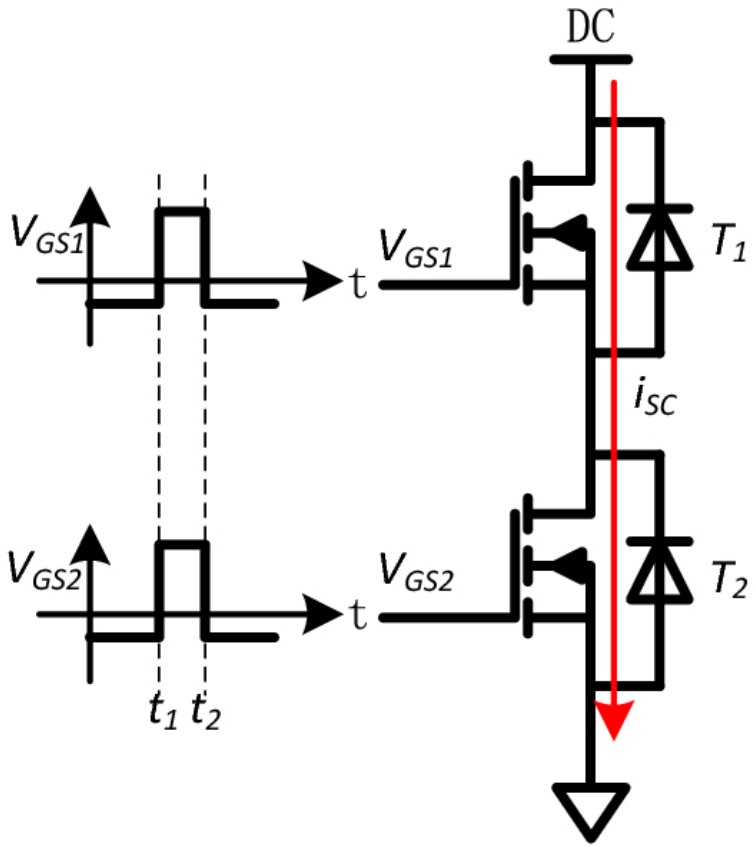
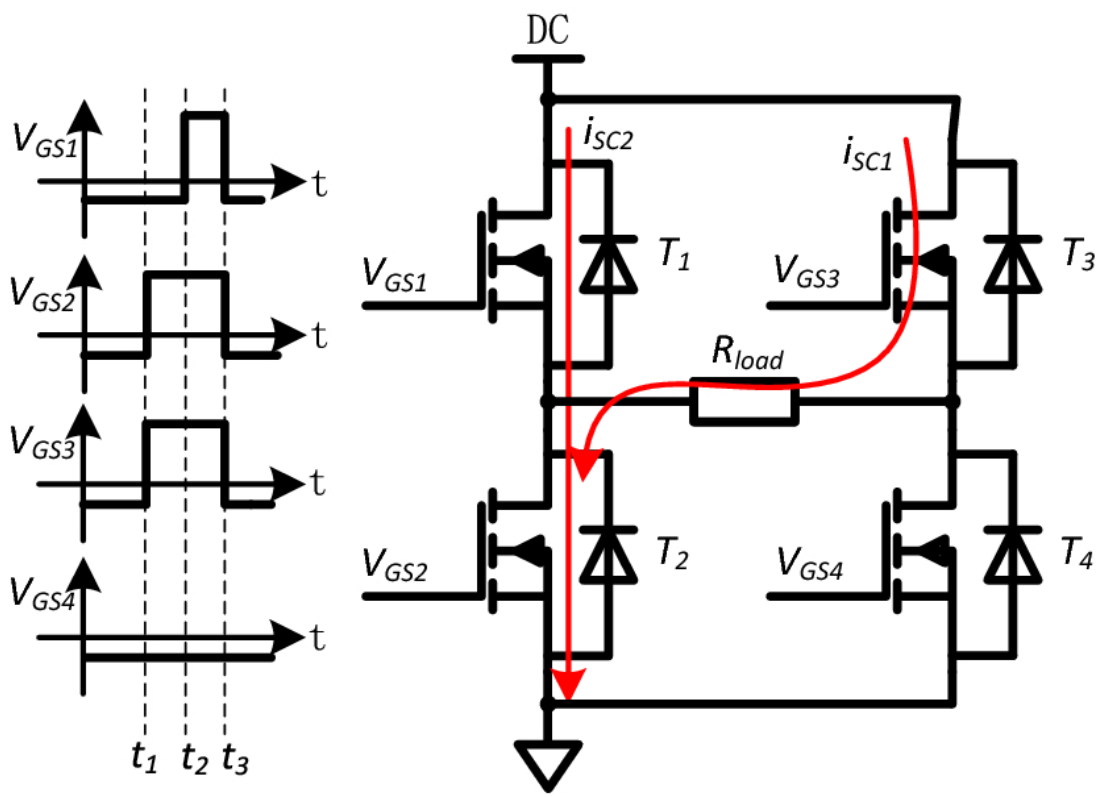
Short Circuit Failure Basic

Type 1: Hard Switching Fault (HSF)

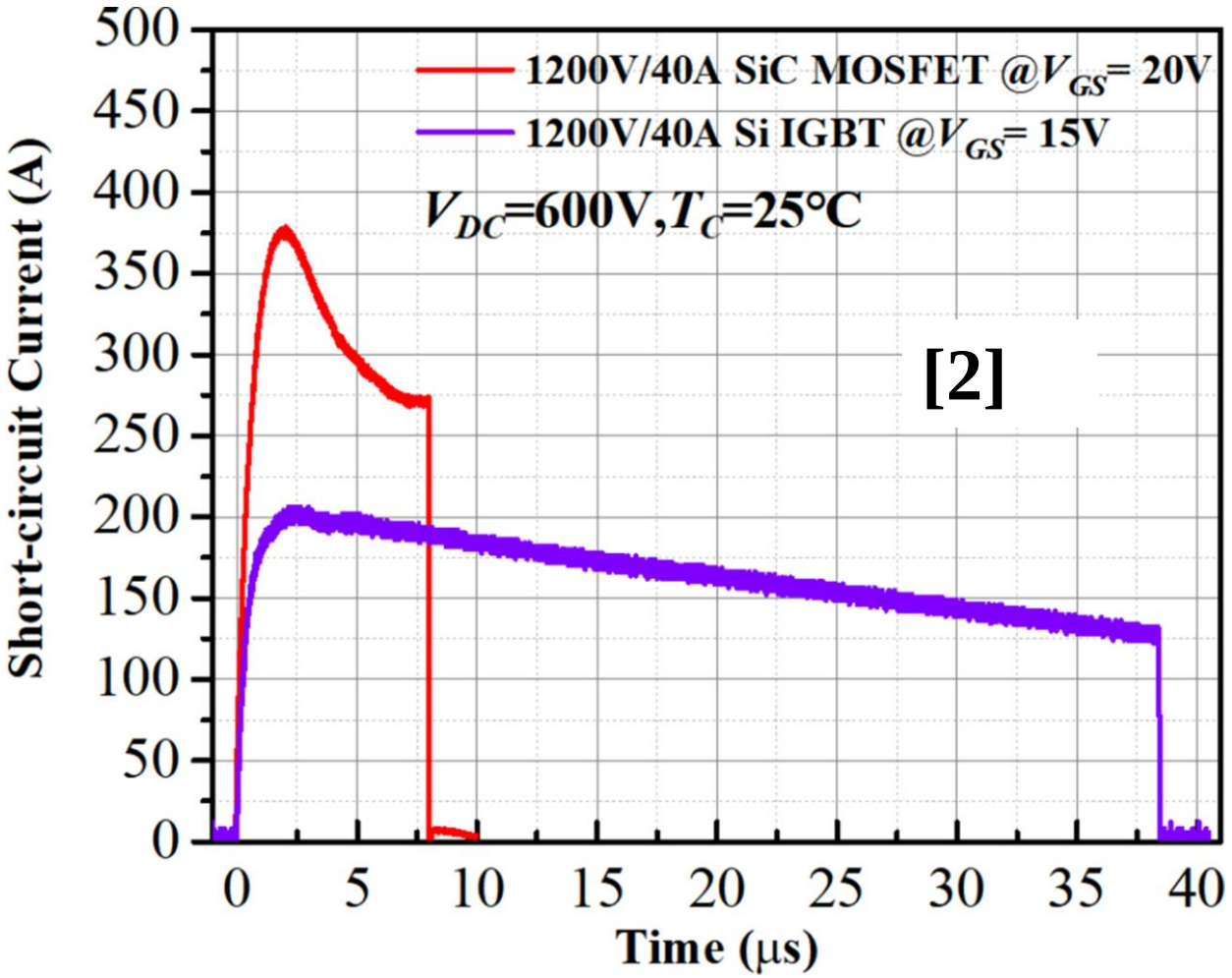


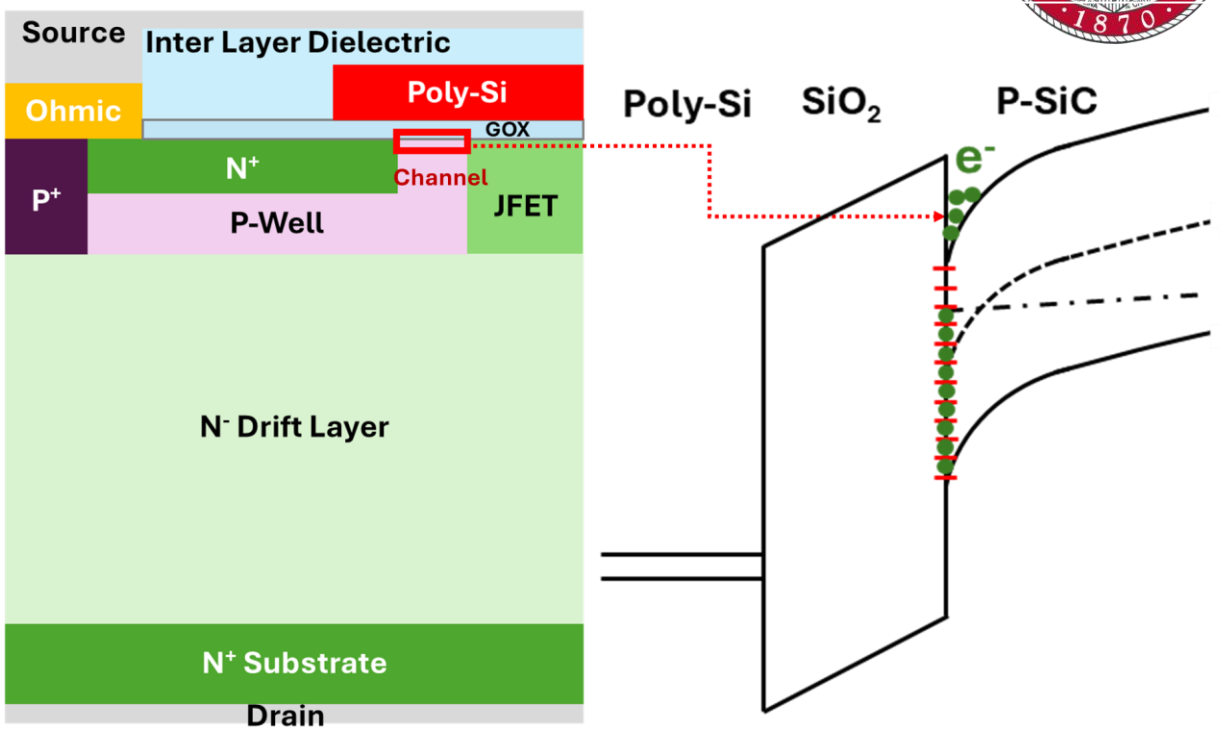
Type 2: Fault Under Load (FUL)



[1] Wang, Z., Tong, C. & Huang, W. Short-circuit protection method for medium-voltage SiC MOSFET based on gate–source voltage detection. J. Power Electron. 20, 1066–1075 (2020).

SiC MOSFET vs Si IGBT Short Circuit Withstand Time

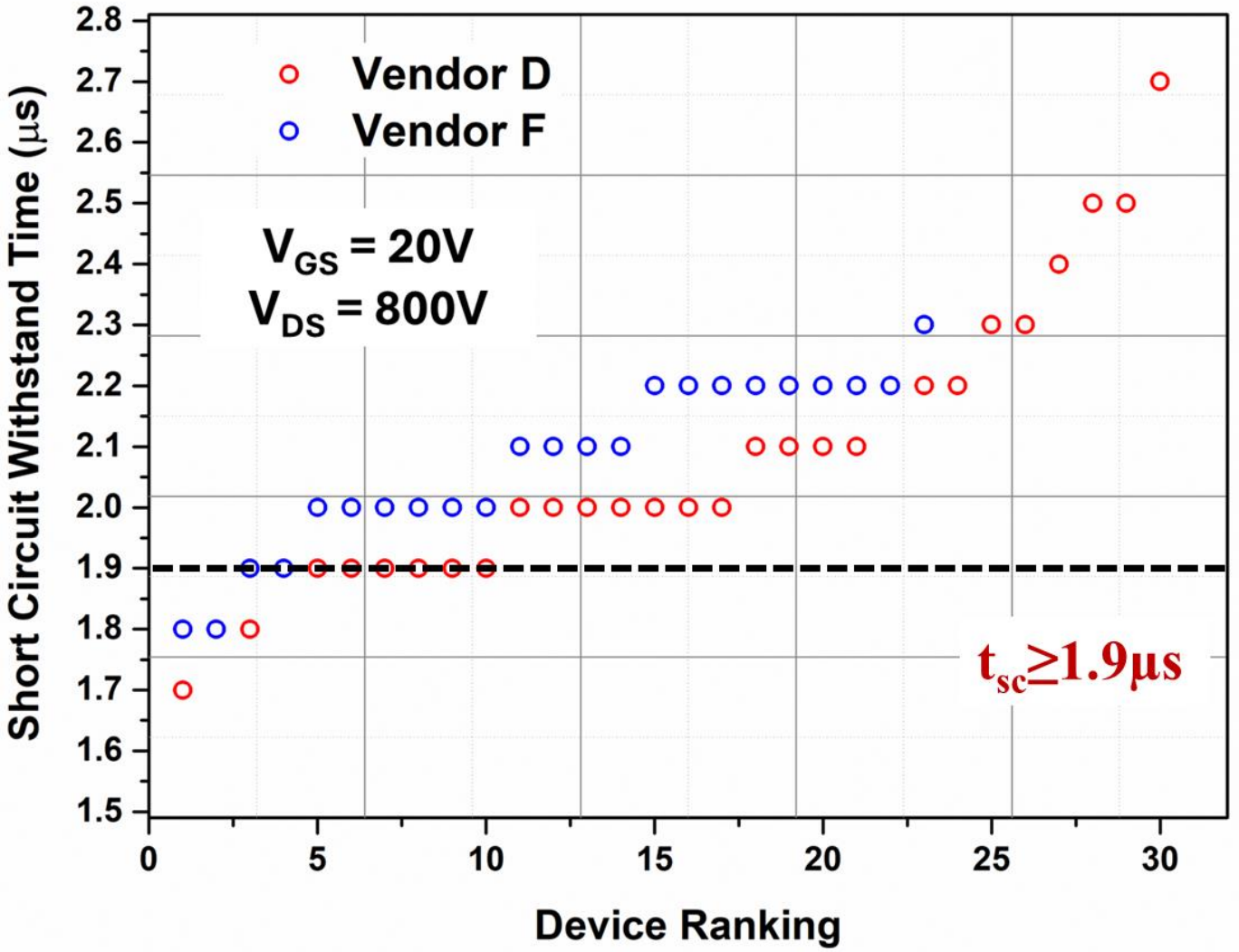




$$R_{CH} \approx \frac{L_{ch}}{W} \frac{t_{ox}}{\mu_n \varepsilon_{SiO_2}(V_{GS} - V_{th})}$$

[2] Wang, Jun, and Xi Jiang. "Review and analysis of SiC MOSFETs' ruggedness and reliability." *IET Power Electronics* 13, no. 3 (2020): 445-455.

SCWT Variation in Commercial SiC 1.2kV Planar Devices



- Channel misalignment causes the variation in SCWT [3].

[3] S. Nayak *et al.*, "Non-isothermal simulation of SiC DMOSFET short circuit capability," *Japanese Journal of Applied Physics*, vol. 61, no. 6, 2022.

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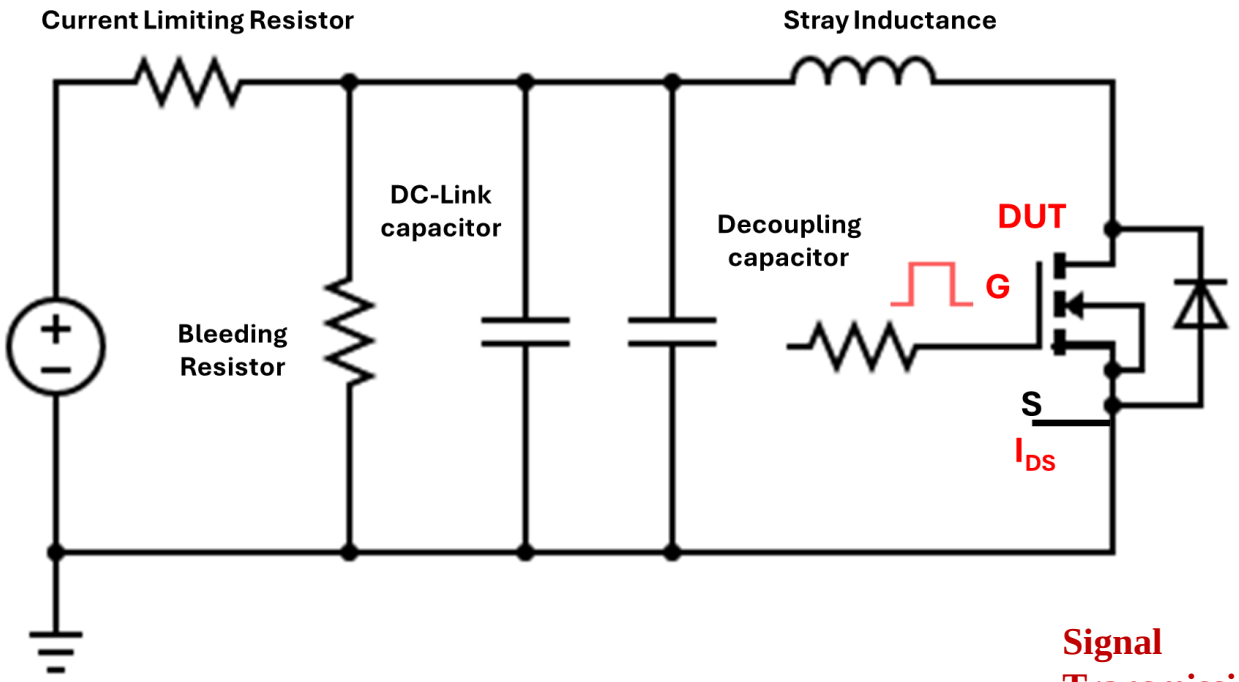
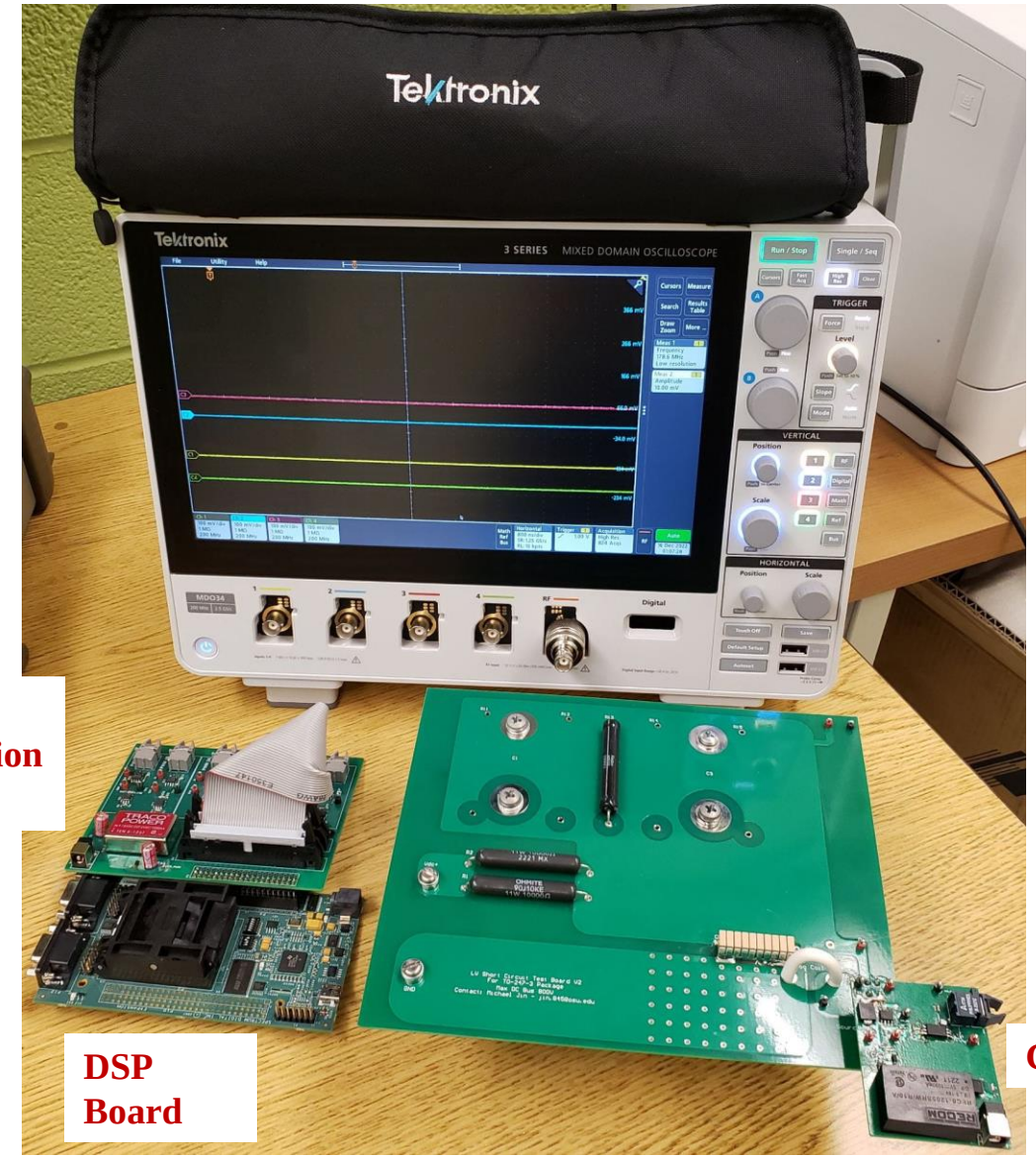
Short Circuit Test Setup





- $V_{GS\text{-}on}$ = 20V
- $V_{GS\text{-}off}$ = 0V
- V_{DS} = 800V
- $t_{pulse\text{-}start}$ = 0.5µs followed by Δt_{pulse} = 0.1µs until failure.

Device Details

Vendor	Vendor D	Vendor F
Device Type	Planar	Planar
Rated Voltage (kV)	1.2	1.2
Rated Current (A)	20	7.6
Drain-Source On Resistance (mΩ)	189	350
Number of Devices	30	23

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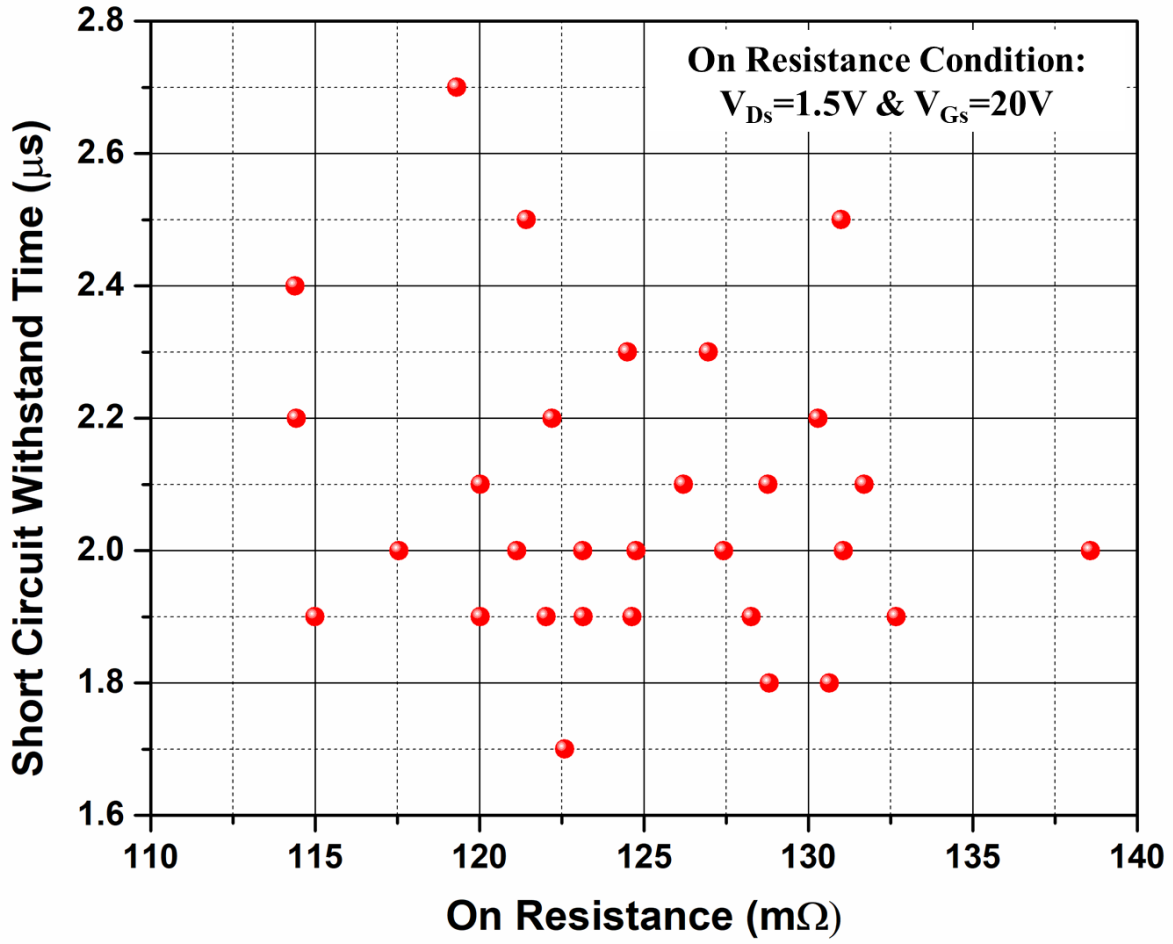
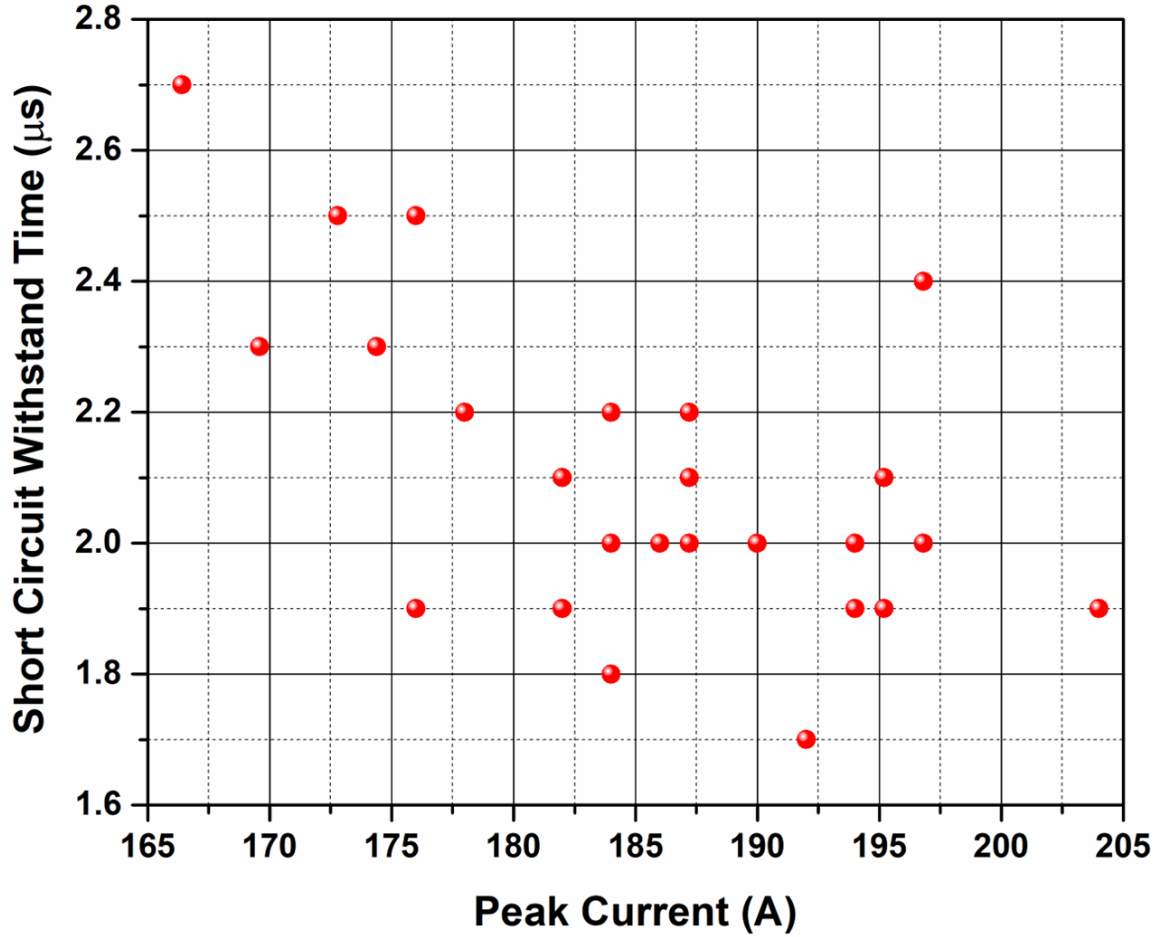
- ❑ Summary

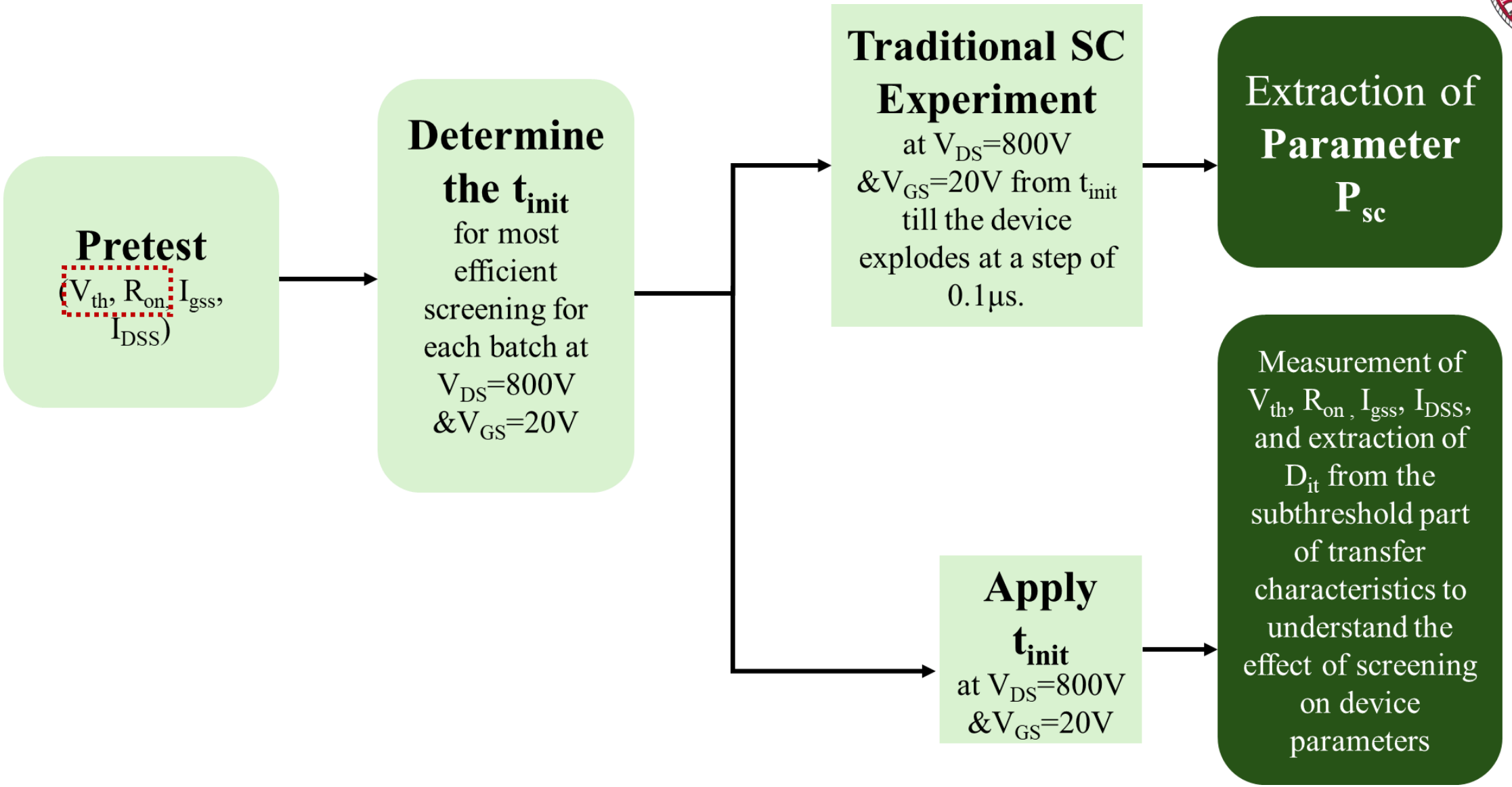
Screening Using Traditional Static Parameters



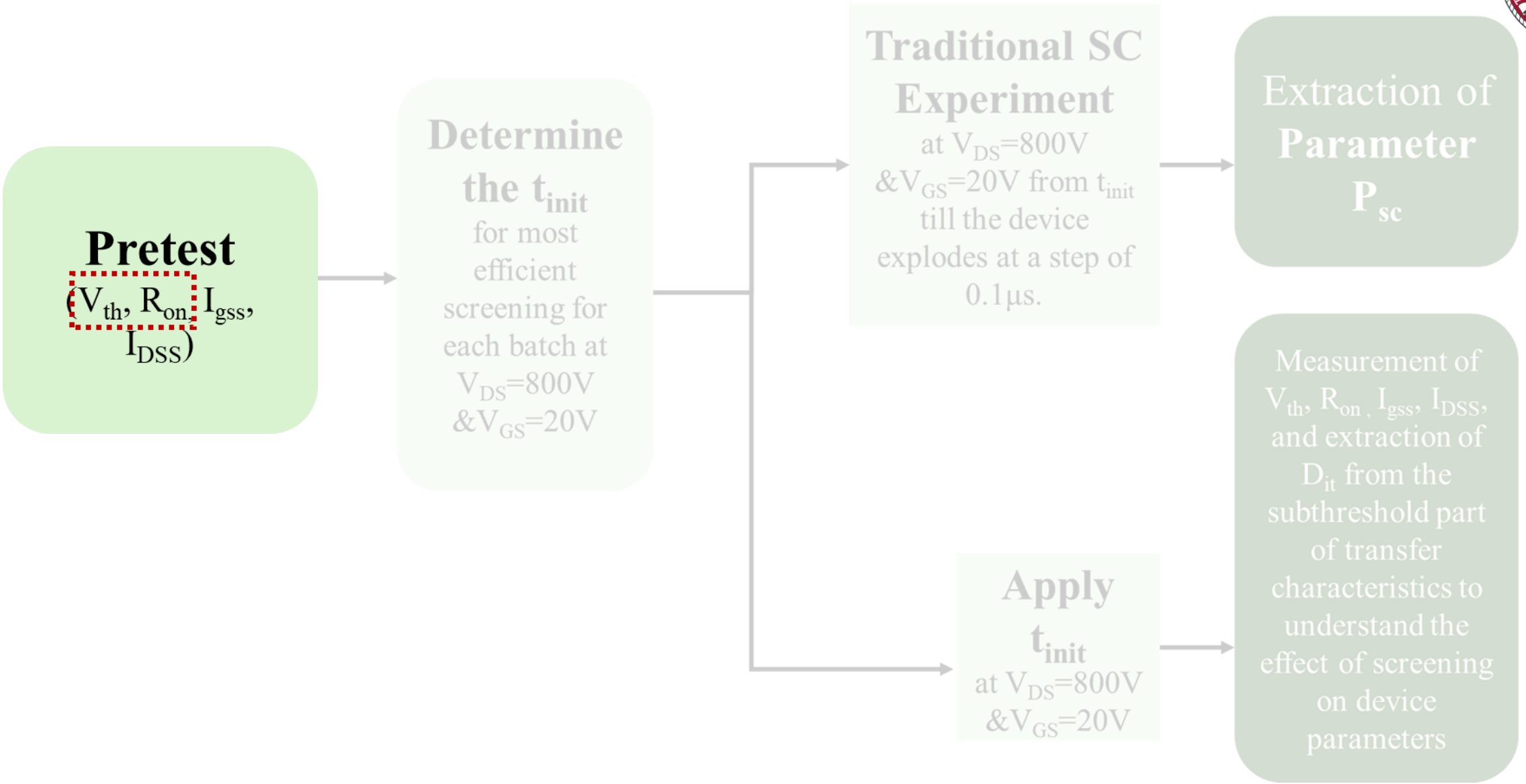


No direct correlation can be established.

Novel Short Circuit Screening Methodology

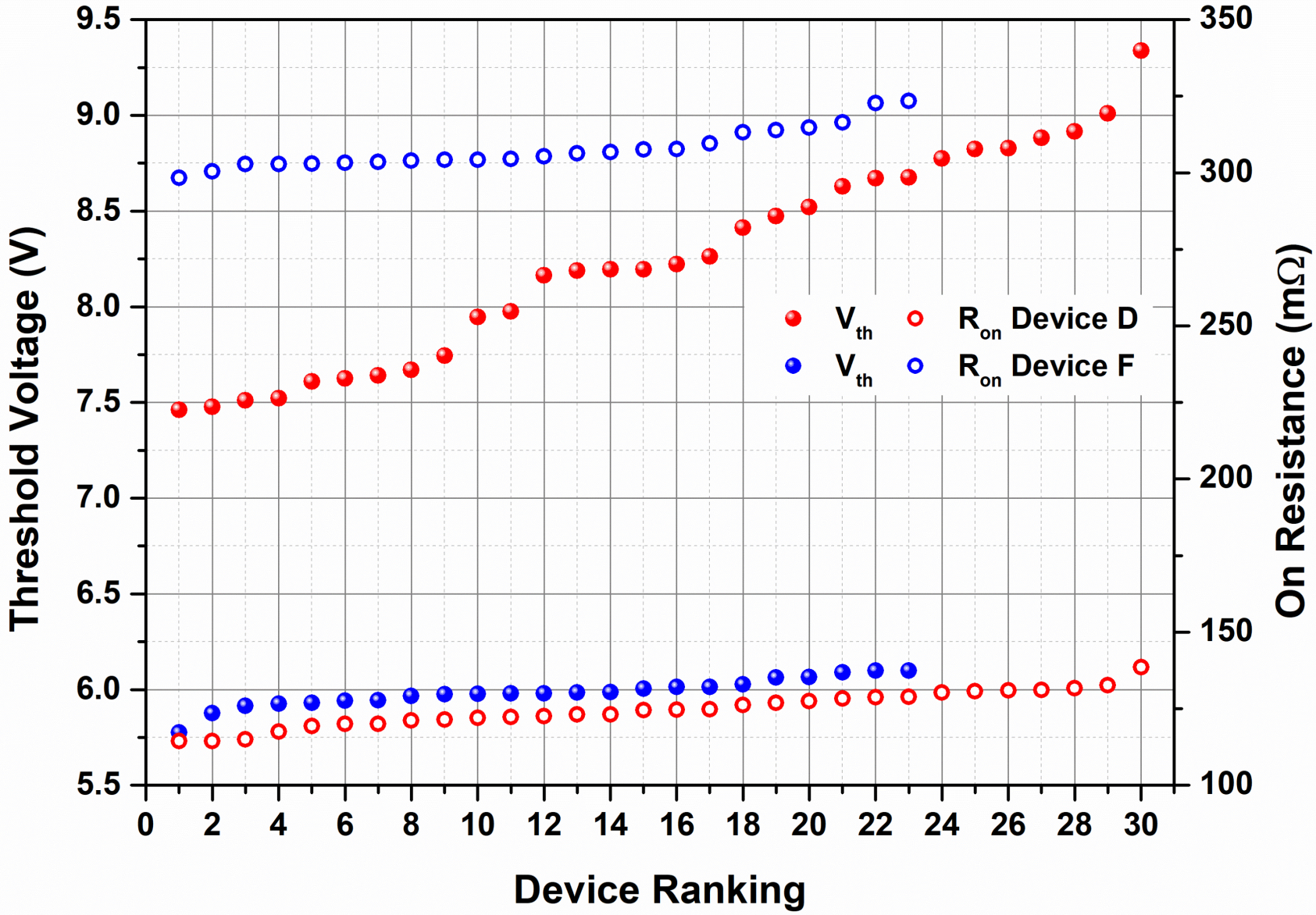


Step 1: Pretest

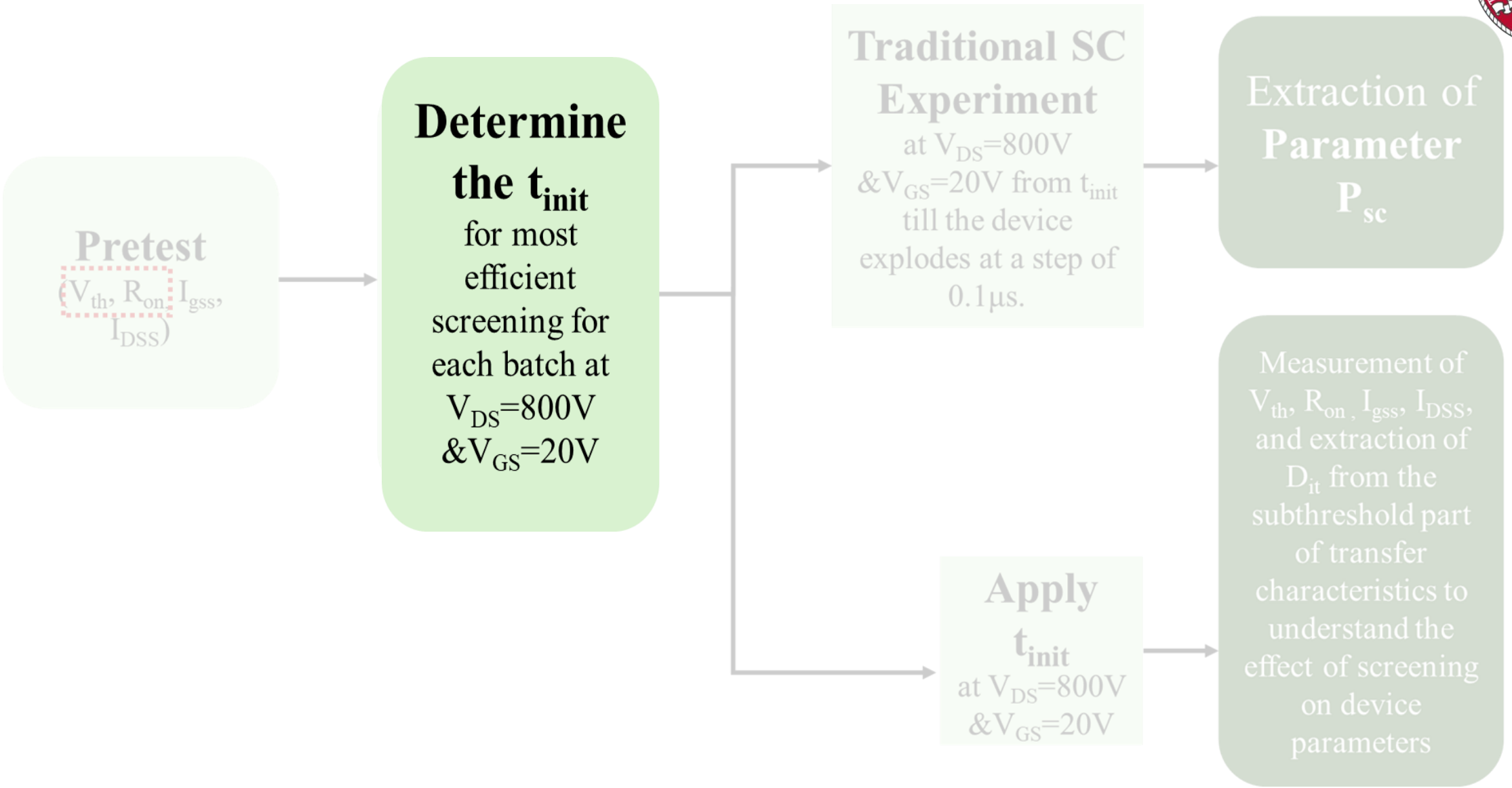


Variation of Threshold Voltage and On-Resistance

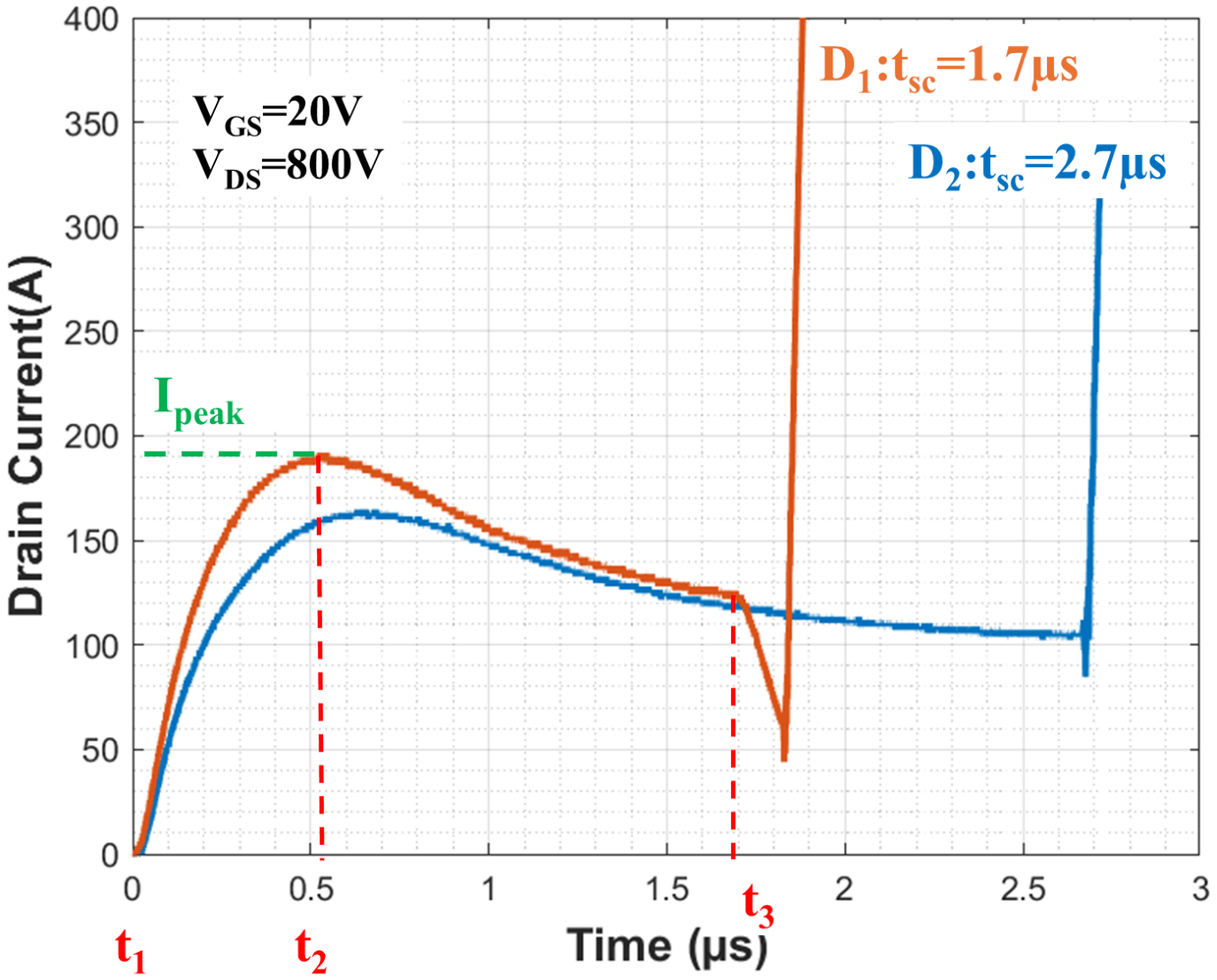
Threshold Voltage:
Linear Extrapolation Method
V_{DS} = 100mV
On Resistance:
V_{GS} = 20V; V_{DS} = 1.5V

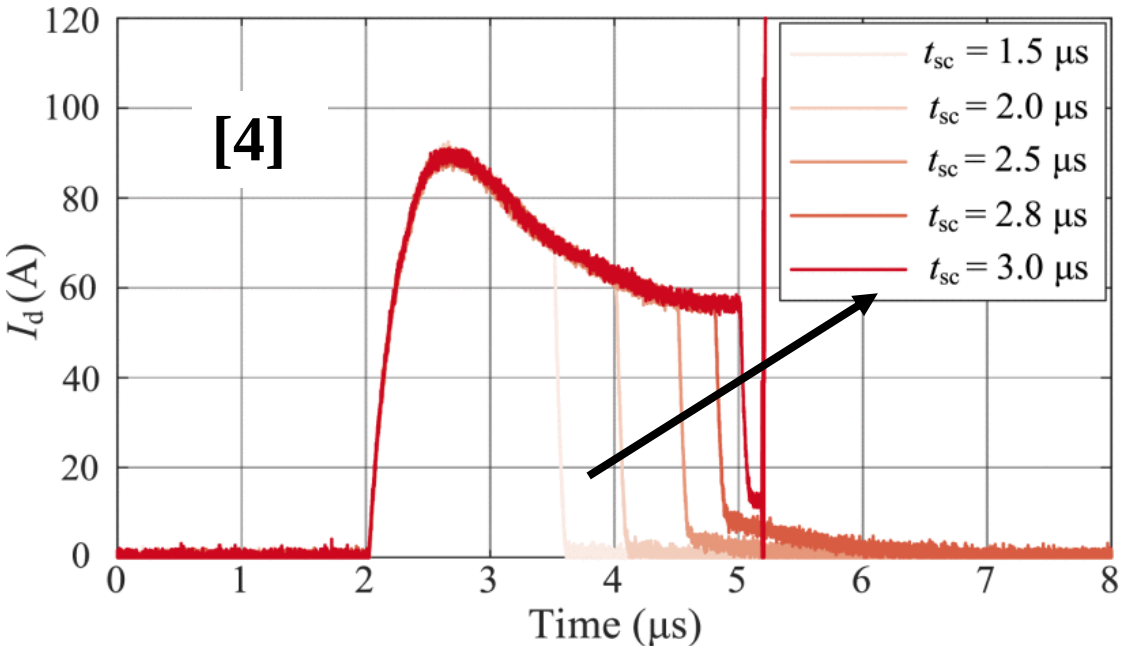


Step 2: Determine the t_{init}



t_{init} Determination





- With the increase in t_{pulse} tail current increases.
- Tail current results in thermal runaway.
- t_{init} should show the tail current effect.
- $t_{init} < t_{scmin}$
- **$t_{init} = t_{scmin}$-0.2µs**

[4] M. Zhang et al.,"Short Circuit Protection of Silicon Carbide MOSFETs: Challenges, Methods, and Prospects," in *IEEE Transactions on Power Electronics*, vol. 39, no. 10, pp. 13081-13095, Oct. 2024

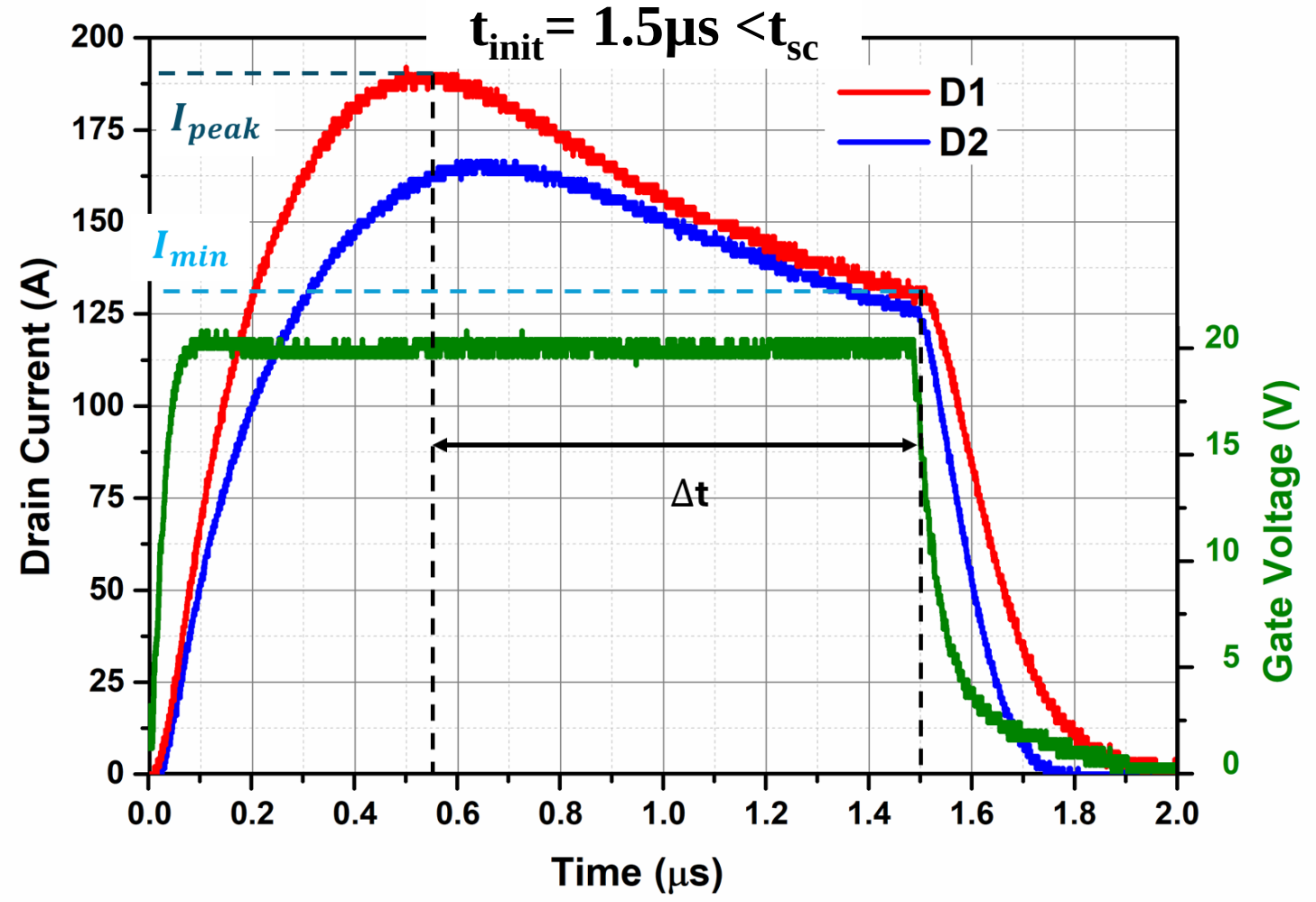
Step 3: Extraction of Screening Parameter

Traditional SC Experiment

at V_{DS}=800V &V_{GS}=20V from t_{init} till the device explodes at a step of 0.1µs.

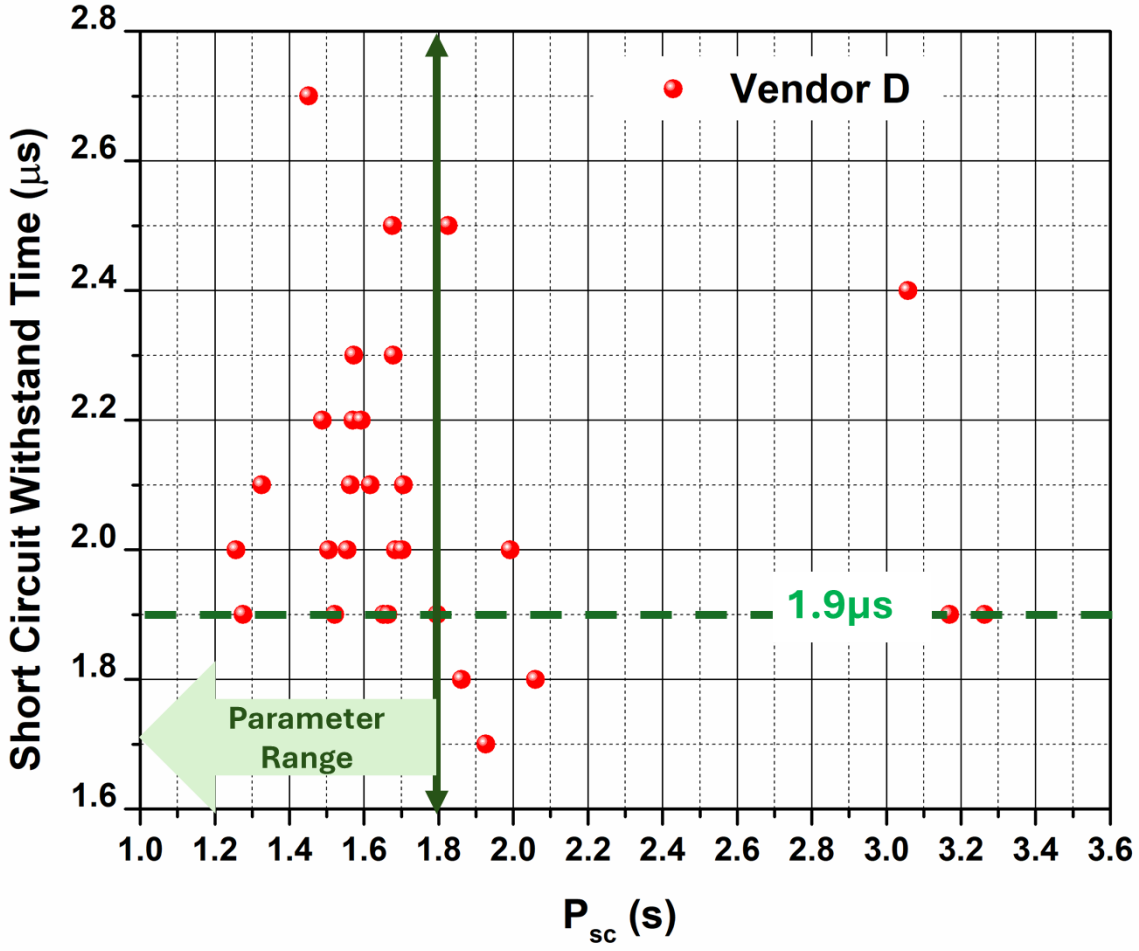
Extraction of **Parameter P_{sc}**

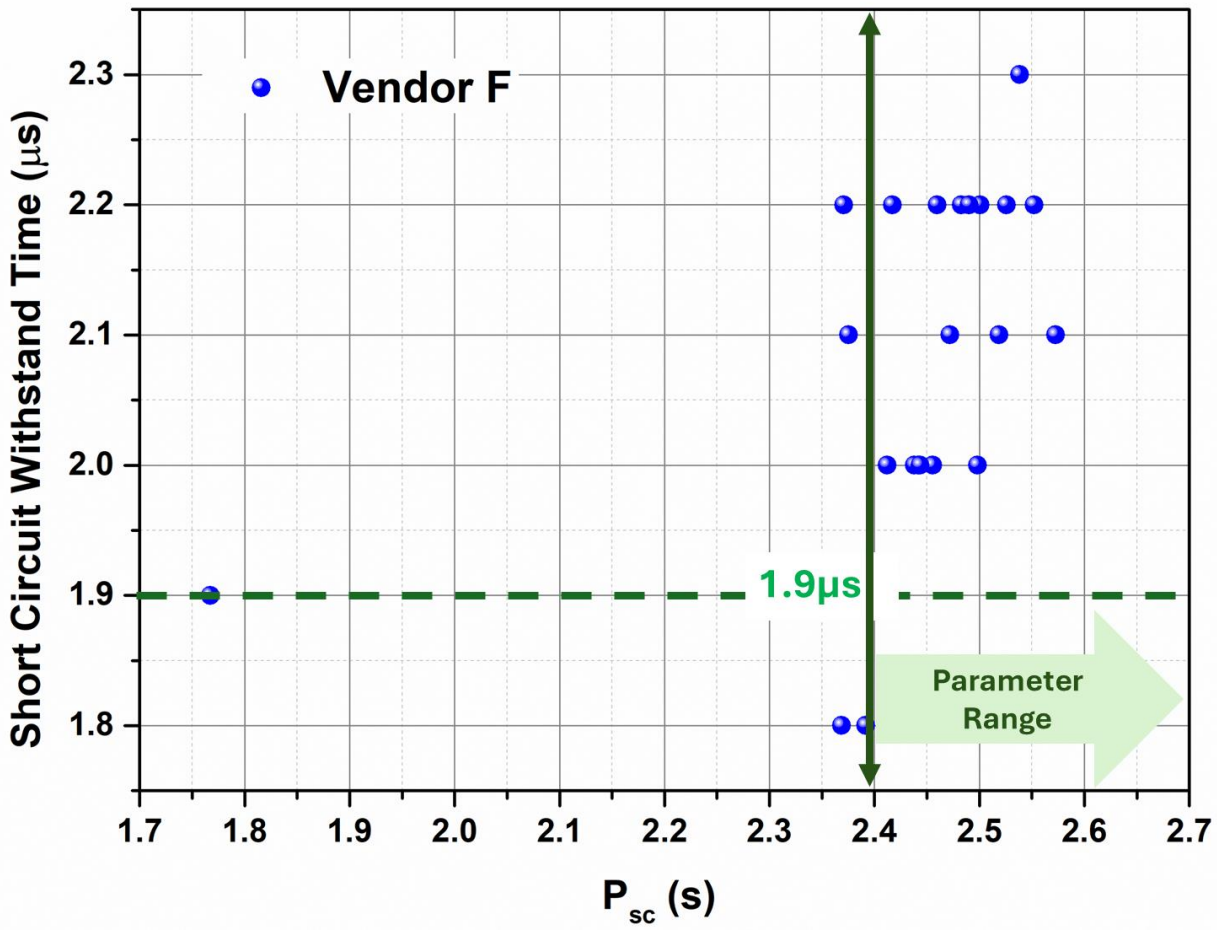
Understanding the Drain Current Behaviour



- Reduction in Drain current after I_{peak} indicates the reduction in mobility due to high temperature.
- **slope** $= \frac{\mathbf{I_{peak} - I_{min}}}{\mathbf{\Delta t}}$ can be correlated with this mobility reduction effect.

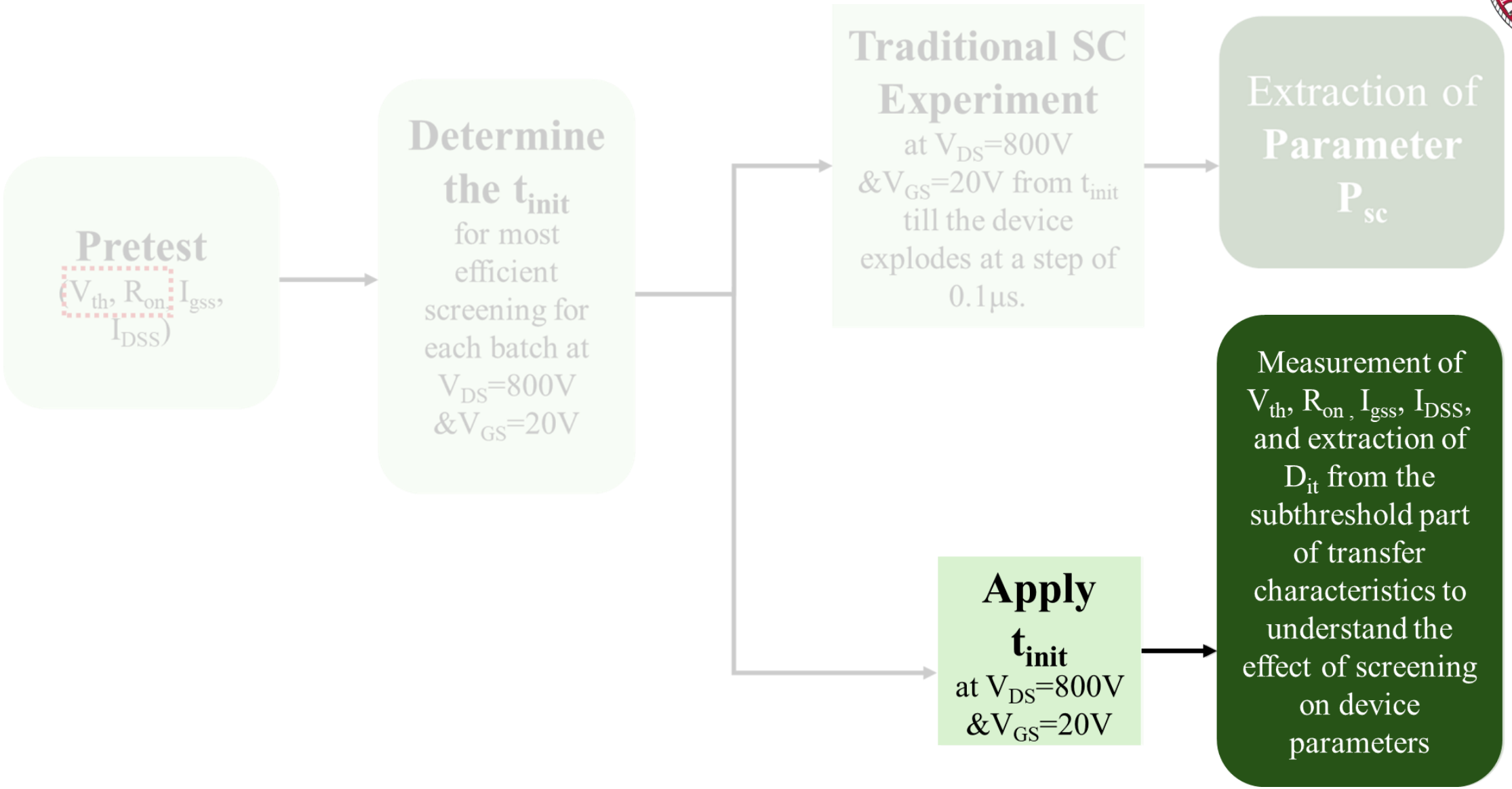
P_{sc} Distribution for Vendor D and Vendor F





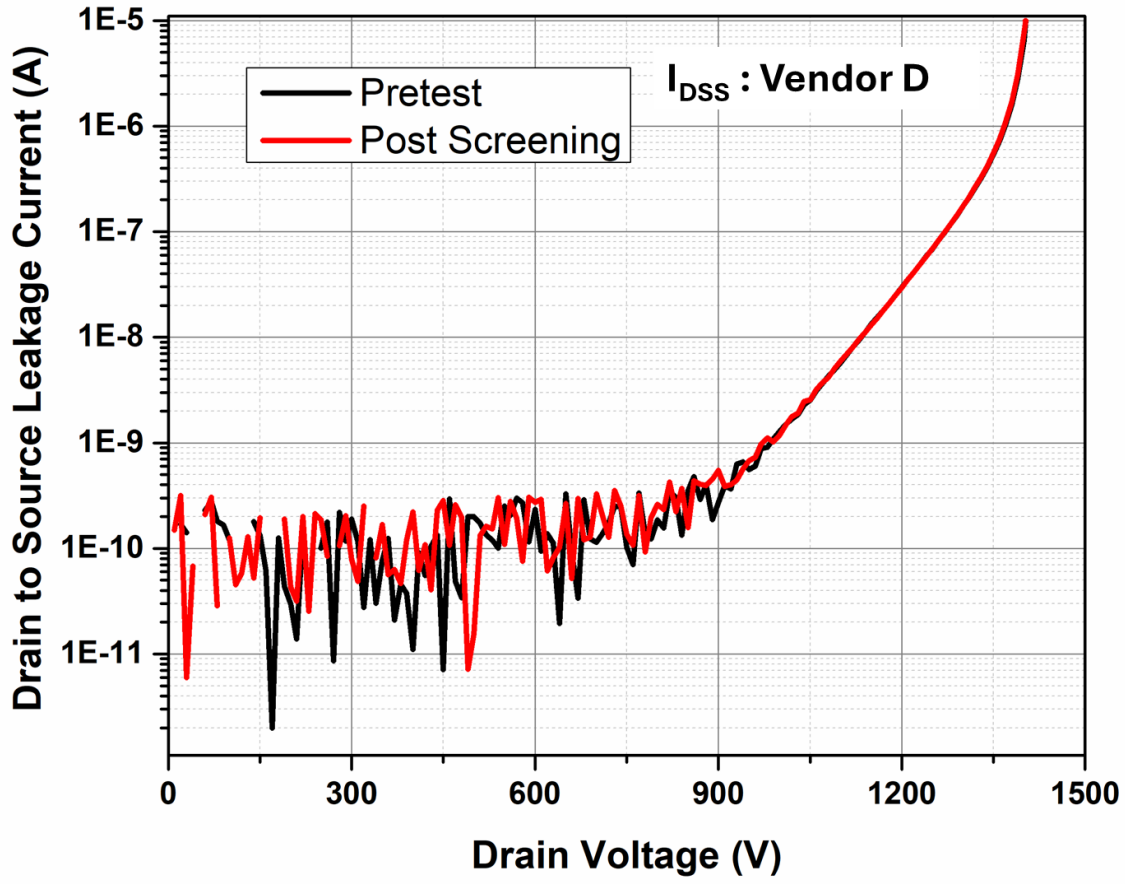
- **Parameter (Psc)** $= \frac{\mathbf{I_{peak}}}{\mathbf{slope}}$ where slope $= \frac{I_{peak} - I_{min}}{\Delta t}$.
- **For $t_{sc} \geq 1.9\mu s$ P_{sc} for Vendor D $\leq 1.8s$ and Vendor F $\geq 2.4s$.**

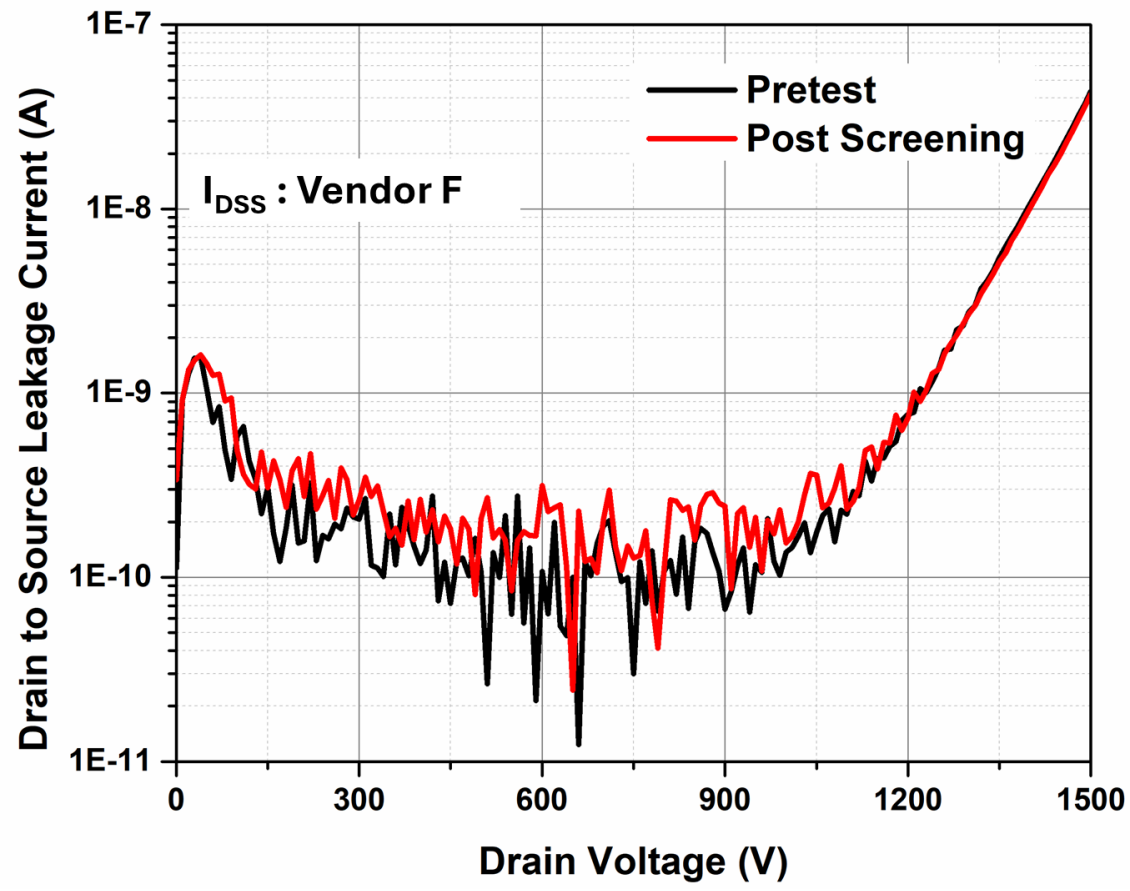
Step 4: Influence of Screening on Device Parameters



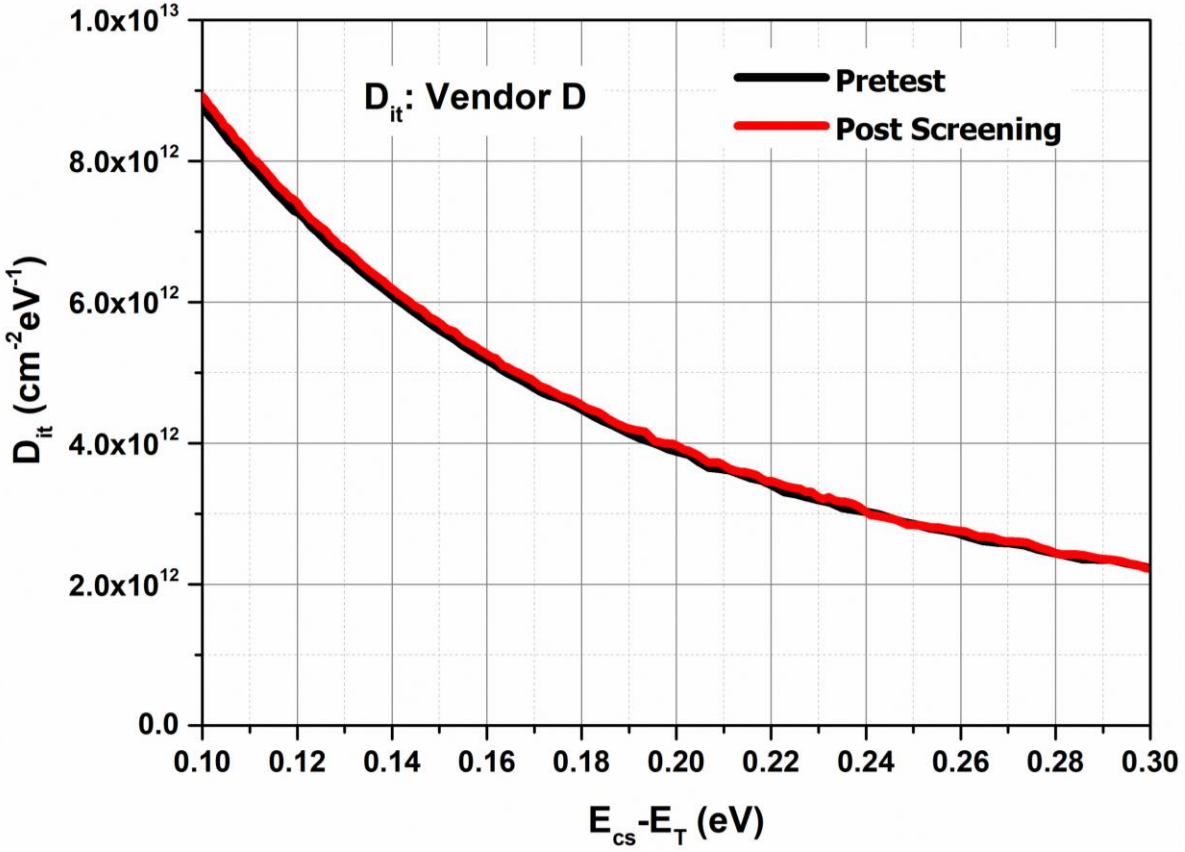
V_{th}, R_{on}, I_{gss}, and I_{DSS} Variation due to Screening

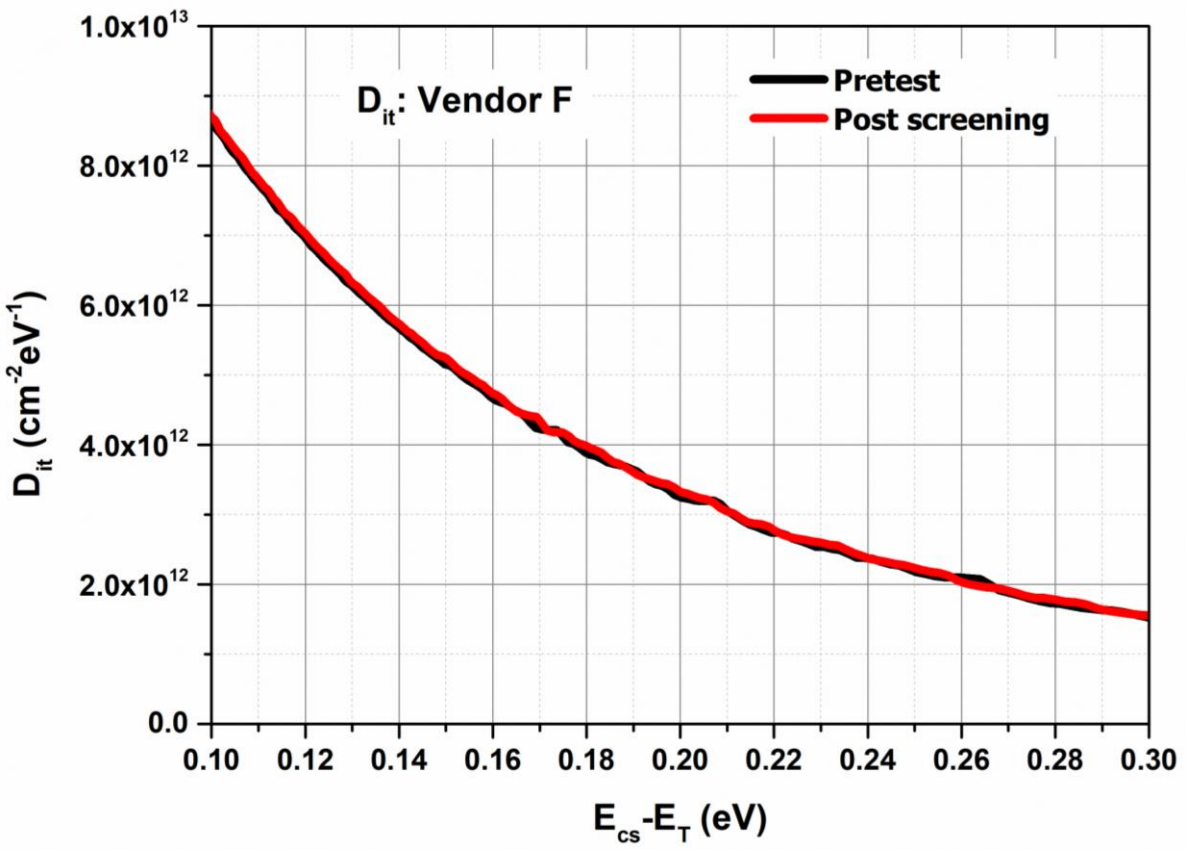
Vendor	V_{th} (V)		R_{on} (mΩ) (V_{GS} = 20V & V_{DS} = 1.5V)		Igss (nA) at V_{GS} = 30V	
	Pretest	Post-screening	Pretest	Post-screening	Pretest	Post-screening
D	7.2	7.2	116.25	116.25	0.081	0.051
F	6.11	6.12	318.2	321.1	27.5	27.1





Room Temperature D_{it} Study





- D_{it} extracted using the subthreshold slope method at room temperature (RT=300K) [5].

No degradation of devices due to screening.

[5] S. Yu, M. H. White and A. K. Agarwal, "Experimental Determination of Interface Trap Density and Fixed Positive Oxide Charge in Commercial 4H-SiC Power MOSFETs," in *IEEE Access*, vol. 9, pp. 149118-149124, 2021.

Outline

- ❑ **Background and Motivation**
  - Short Circuit Failure Basic
  - SiC MOSFET vs Si IGBT Short Circuit Withstand Time
  - SCWT Variation in Commercial SiC 1.2kV Planar Devices
- ❑ **Experiment Procedure and Samples**
  - Short Circuit Test Setup
  - Device Details
- ❑ **Novel Short Circuit Screening Methodology**
- ❑ **Summary**

Summary

- Commercial SiC MOSFETs show SCWT variation across the batch with the same lot number due to slight channel misalignment.

- To reliably remove devices with lower SCWT, a novel screening parameter $P_{sc}(s)$ has been introduced that captures the temperature-dependent mobility.

- To successfully remove devices with $t_{sc} \leq 1.9\mu s$ calibrated P_{sc} for Vendor D $\leq 1.8s$ and Vendor F $\geq 2.4s$.

- The proposed screening method can remove devices with lower SCWT without damaging the reliable ones.

Reduces the risk of failure in the field.

Thank You for Your Attention!

Any Questions?