Coherent/II-VI Foundation Mini-Conference 2025, May 19.

Unique electron trapping and its impacts on electron mobility in SiC n-channel MOSFETs

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Outline of this talk

1. Background and purpose of this study

2. Device fabrication and measurements

3. Unique carrier trapping near SiC MOS interfaces

4. Carrier scattering and physics-based model of SiC MOSFETs

5. Summary

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SiC MOSFETs: next-generation low-loss and high-voltage power devices

SiC MOSFETs in practical use

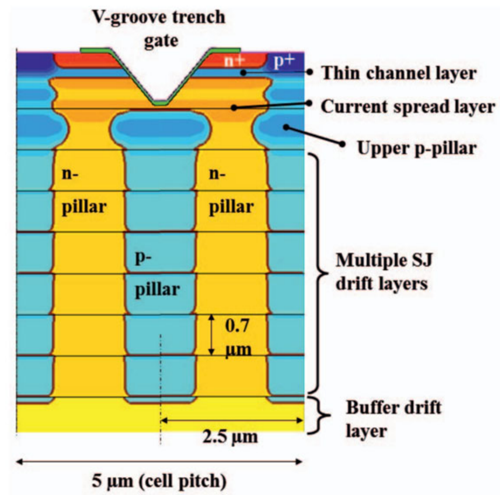
EV **Tesla Model 3**

Train **JR “Shinkansen”**

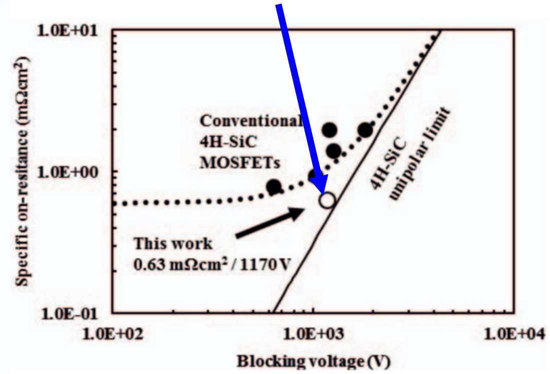
Remarkable energy saving

https://www.statista.com/chart/16948/total-number-of-premium-cars-sold-in-the-us/
https://jr-central.co.jp/news/release/nws001685.html

Research on the highest-performance SiC MOSFET



Lowest on-resistance (by AIST)



Super Junction V-Groove Trench MOSFET (AIST) [1]

1170 V – 0.63 mΩcm^2

[1] T. Masuda *et al.*, *IEDM Tech. Dig.* (2018), p. 177.

The main issue in SiC MOSFETs

A high density of **interface traps** exists near the MOS interface (origin is still unclear)

Energy distribution of interface trap density (D_{it})

- D_{it}: increase exponentially towards E_C
- D_{it} near E_C: **∼10^{14} cm^{-2} eV^{-1}**
  … 1000 times higher than Si MOS

Performance degradation caused by high D_{it}

E_F approaches E_C in the on-state of MOSFETs

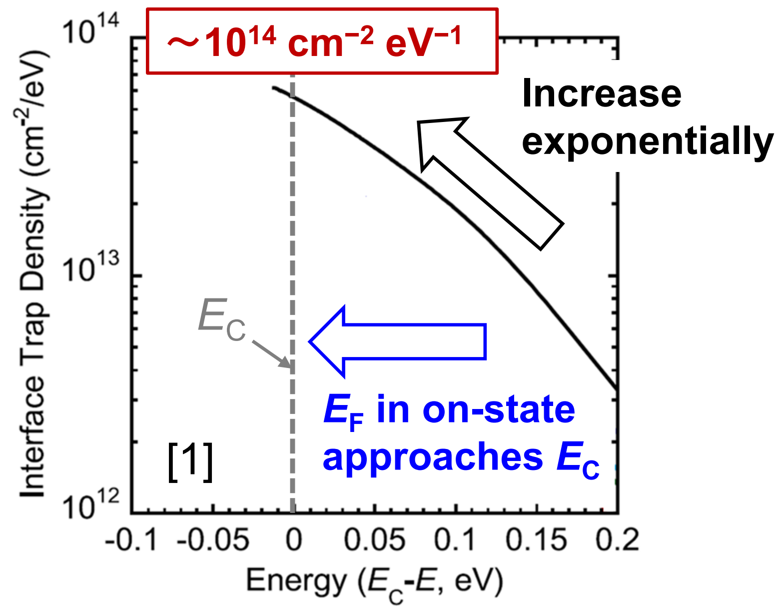
Extremely high D_{it} near E_C

1. Severe electron trapping
2. Coulomb scattering

Main reason for the low channel mobility in SiC MOSFETs

(μ_{ch} = 20 cm^2/Vs vs. μ_{bulk} = 1020 cm^2/Vs)

D_{it} distribution near E_C
(partially modified quote)



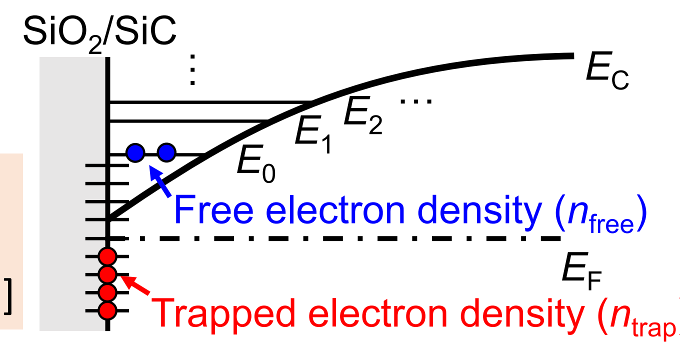
[1] T. Hatakeyama *et al.*, *Appl. Phys. Express* **12**, 021003 (2019).

Impact of interface traps on device characteristics

Relationship of μ_{ch} and μ_{free} in SiC MOSFETs

$$\mu_{ch} = \frac{n_{free}}{n_{free}+n_{trap}}\mu_{free}$$

(In Si MOSFETs: $\mu_{ch} = \mu_{free}$)



- Channel mobility: determines the channel resistance
- Free electron ratio: depends strongly on D_{it}
- Free electron mobility: strongly affected by Coulomb scattering caused by high n_{trap} [1]

μ_{ch}: include **"Trapping"** × **"Scattering"** caused by interface traps

Basic understanding of interface traps: essential for modeling of SiC MOSFETs

However…

There is a lack of comprehensive understanding of interface traps

→ Modeling of SiC MOSFETs is incomplete (a long-standing issue)

[1] K. Ito *et al., Appl. Phys. Express* **16,** 071001 (2023).

Purpose of this study

To distinguish the impacts of trapping and scattering

→ Measurements of n_{free}, μ_{free}, n_{trap} are necessary (not μ_{ch})

$$\mu_{ch} = \frac{n_{free}}{n_{free}+n_{trap}}\mu_{free}$$

trapping scattering

Previous study

Combine **Split *C*—*V*** and **MOS Hall-effect** measurements [1]

Obtain total electron density (n_{total}) | Obtain n_{free} and μ_{free} separately ► $n_{trap} = n_{total} - n_{free}$

($\mu_{Hall} = \mu_{free}$ with Hall scattering factor = 1)

Objective

By the measurement and calculation of n_{free}, μ_{free}, n_{trap}

- Obtain a comprehensive understanding of the interface traps
- Elucidate electron trapping and scattering mechanisms in SiC MOS channels

Establish a physics-based model for SiC MOSFETs based on a comprehensive understanding of electron trapping and scattering phenomena

[1] T. Hatakeyama *et al.*, *Appl. Phys. Express* **10**, 046601 (2017).

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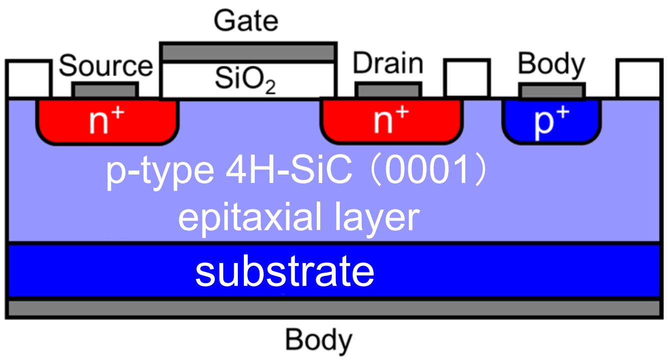
Device fabrication and measurements

Device fabrication



Gate oxides

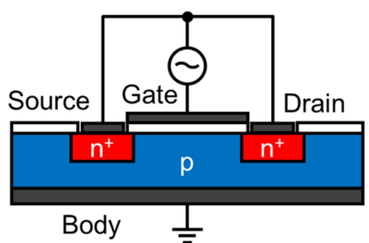
Dry oxidation → NO annealing (standard process)
(Oxide thickness: 42 ∼ 50 nm)

P-body doping concentrations (N_A)

7×10^{14}, 3×10^{15}, 3×10^{16}, 3×10^{17}, 1×10^{18} cm^{-3}

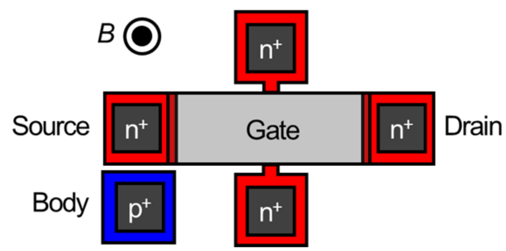
Measurements and extraction of n_{trap}

Split C–V measurements



Measurement of n_{total}

MOS-Hall effect measurements



Measurement of n_{free} and μ_{free}
(Hall scattering factor = 1)

Extraction of n_{trap}

$$n_{trap} = n_{total} - n_{free}$$

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Possible origins of interface traps

(1) Near-interface oxide traps (NITs)

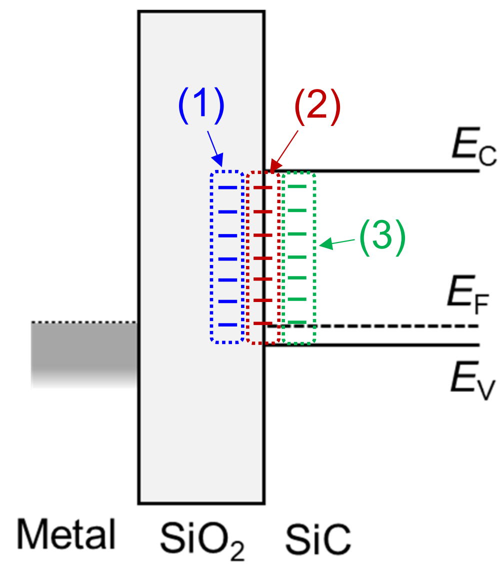
- C defects [1] (C_O=C_O [2], Si_2–C–O [3])
- Intrinsic oxide defects

(2) Traps at the MOS interface

- C defects (C clusters [1,2], C-C [4])
- Dangling bonds [5]

(3) Traps in SiC

- Conduction band fluctuations [6, 7]
- C defects ($(C_2)_{Si}$ [8])

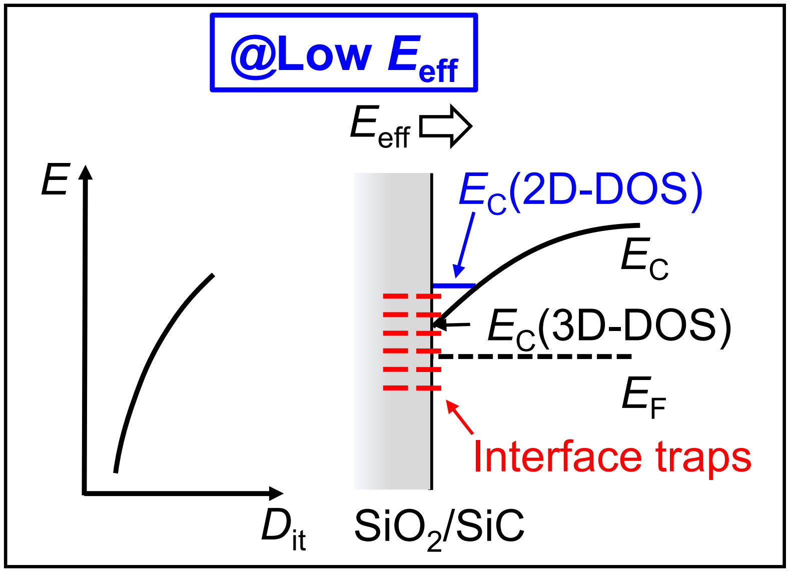


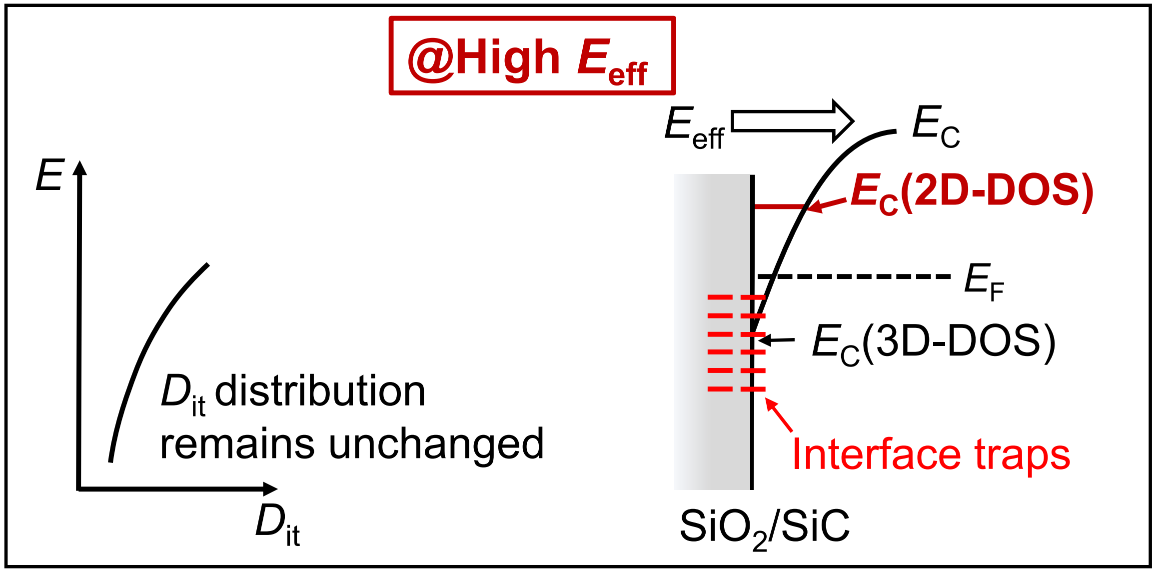
Where are the interface traps primarily located?
... Important information for the modeling of SiC MOSFETs

[1] V. V. Afanasev *et al.*, *Phys. Status Solidi A* **162**, 321 (1997).
[2] P. Deák *et al.*, *J. Phys. D: Appl. Phys.* **40**, 6242 (2007).
[3] F. Devynck *et al.*, *Phys. Rev. B* **84**, 235320 (2011).
[4] X. Shen *et al.*, *Appl. Phys. Lett.* **98**, 053507 (2011).
[5] T. Umeda *et al.*, *Appl. Phys. Lett.* **113**, 061605 (2018).
[6] Y. Matsushita *et al.*, *Nano Letters* **17**, 6458 (2017).
[7] H. Yoshioka *et al.*, *AIP Advances* **8**, 045217 (2018).
[8] T. Kobayashi and Y. Matsushita, *JAP* **126**, 145302 (2019).

Quantum confinement effect and D_{it} distribution

Increasing effective field (E_{eff}): enhances the quantum confinement effect



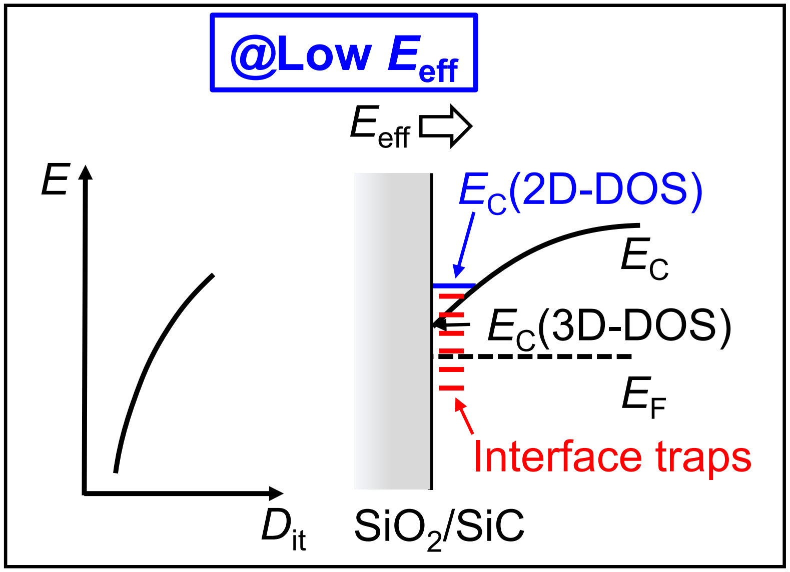


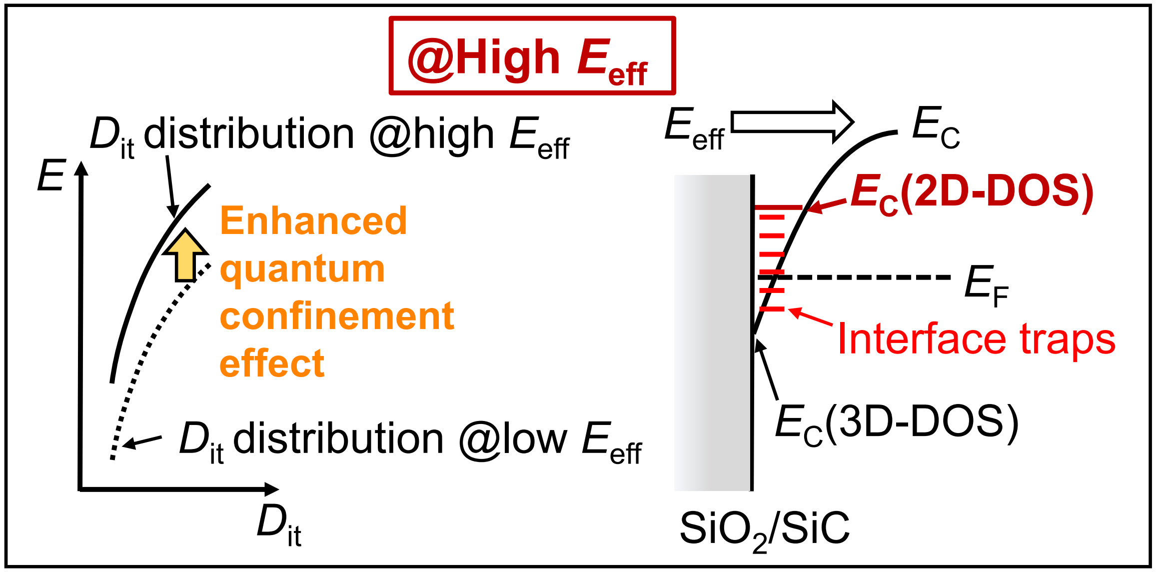
[Case 1] Traps are primarily located <u>within the SiO_2</u> or <u>at the MOS interface</u>:

D_{it} distribution is energetically fixed with respect to E_C(3D-DOS)

Quantum confinement effect and D_{it} distribution

Increasing effective field（E_{eff}）: enhances the quantum confinement effect





[Case 2] Traps are primarily located in SiC:

D_{it} distribution may shift along with E_C(2D-DOS)

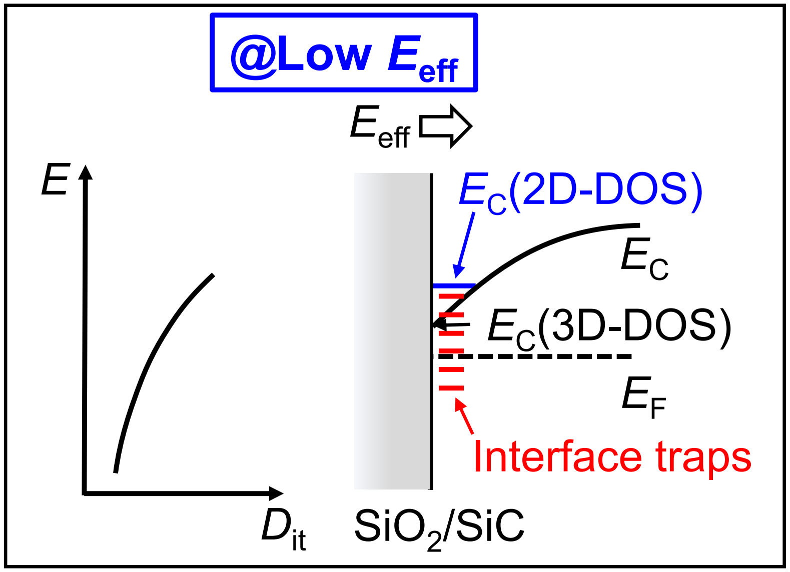
Control of E_{eff}

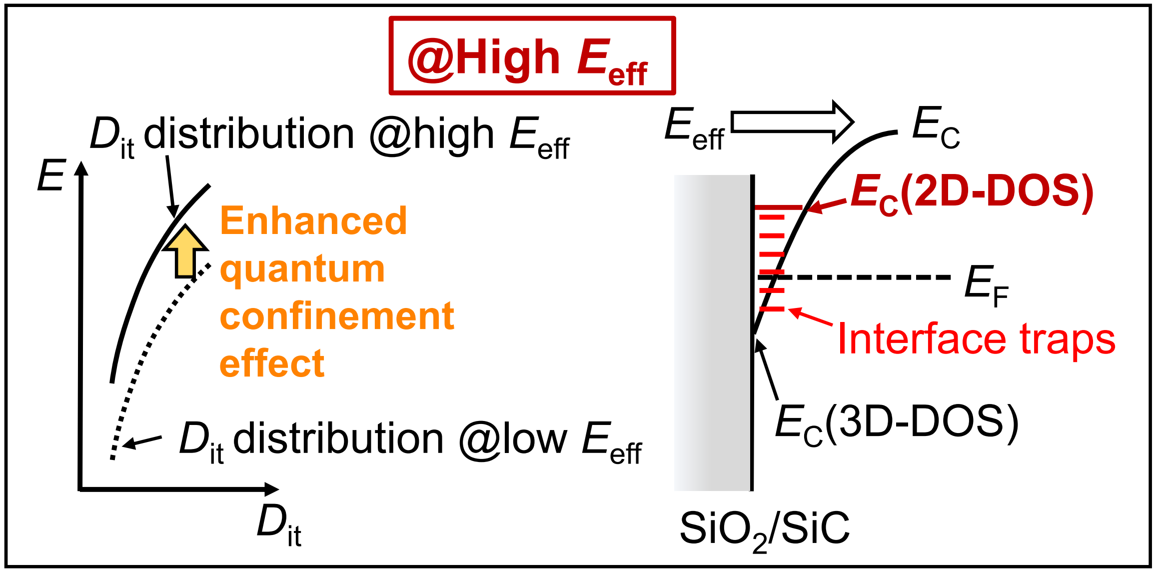
E_{eff} can be controlled by p-body doping concentration (***N_A***) and body bias（***V_{body}***）

$$E_{eff} = \frac{\sqrt{2e\varepsilon_{SiC}\boldsymbol{N_A}(2\psi_B - \boldsymbol{V_{body}})} + en_{free}/3}{\varepsilon_{SiC}}$$

Quantum confinement effect and D_{it} distribution

Increasing effective field（E_{eff}）: enhances the quantum confinement effect





[Case 2] Traps are primarily located in SiC:

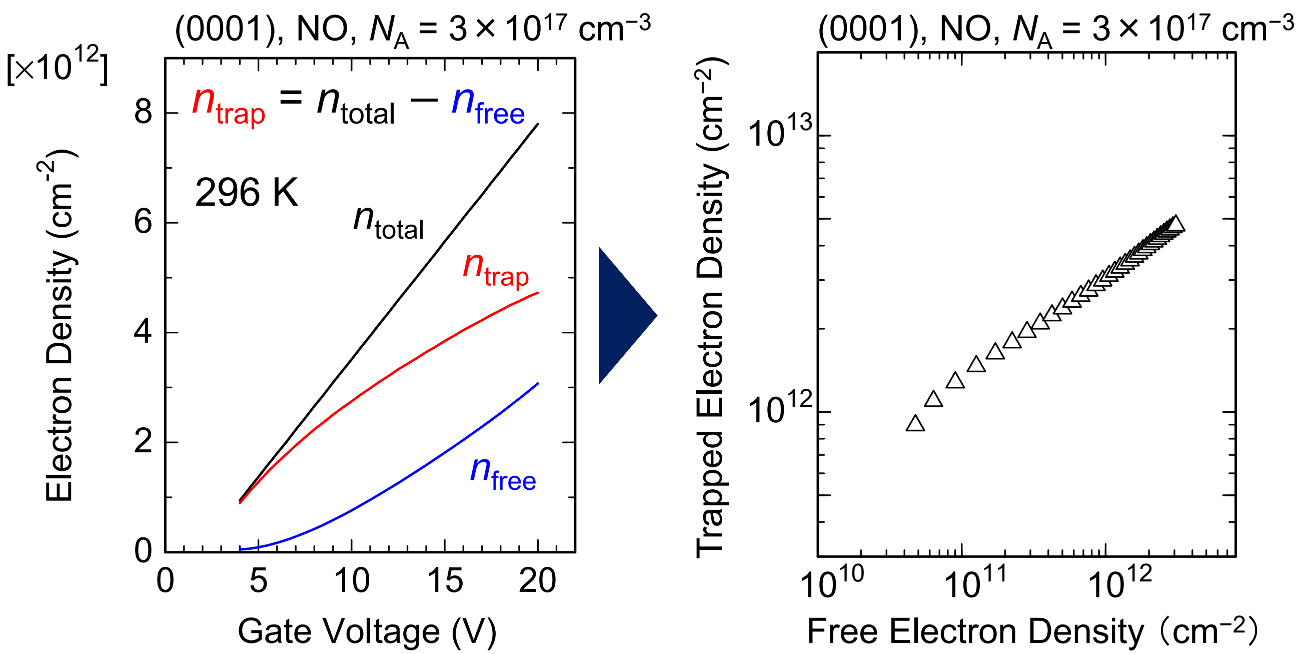
D_{it} distribution may shift along with E_C(2D-DOS)

Clarify where the interface traps are primarily located
by investigating whether the D_{it} distribution shifts along with E_C(2D-DOS)
(by changing N_A and V_{body})

Experimental results and extraction of D_{it} distribution

V_G dependences of electron densities

n_{trap}—n_{free} characteristics



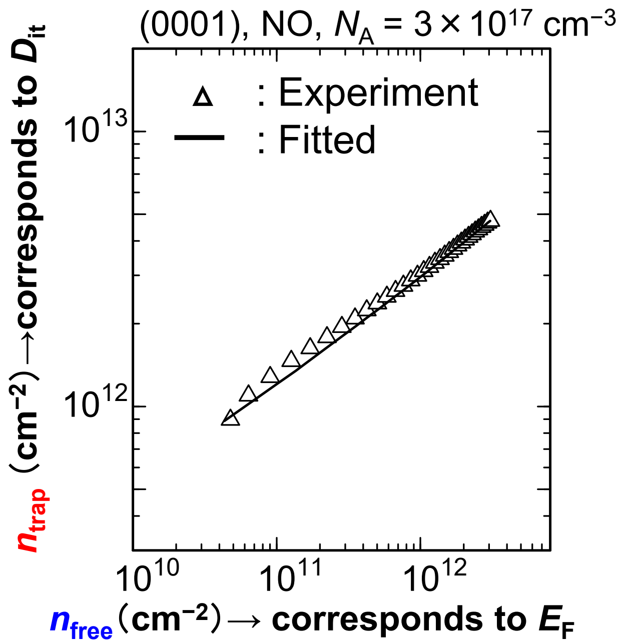
[1] K. Ito *et al.*, *J. Appl. Phys.* **128**, 095702 (2020)

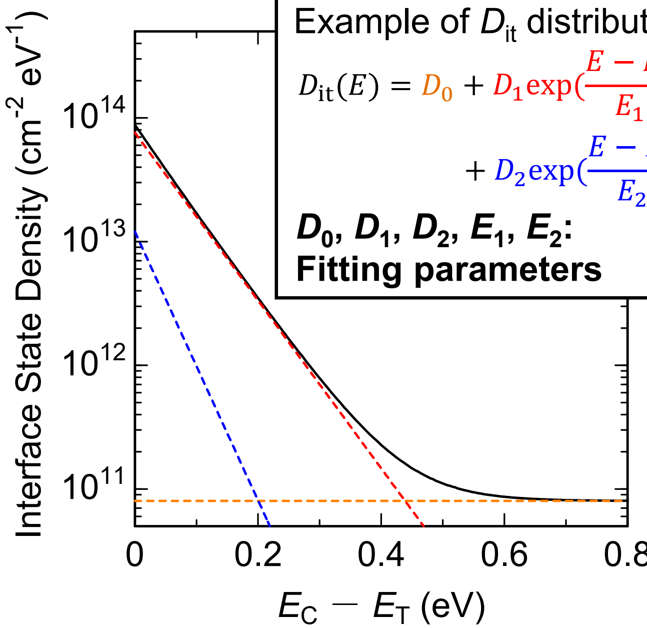
Experimental results and extraction of D_{it} distribution

$$n_{trap} = \int_{E_i}^{\infty} \frac{1}{\exp\left(\frac{E - E_F(n_{free})}{k_B T}\right) + 1} D_{it}(E)\, dE$$

Extraction method

1. Calculate E_F from n_{free} self-consistently [1]
2. Extract D_{it} distributions by reproducing n_{trap}—n_{free} characteristics





Example of D_{it} distribution:

$$D_{it}(E) = D_0 + D_1 \exp\left(\frac{E - E_C}{E_1}\right) + D_2 \exp\left(\frac{E - E_C}{E_2}\right)$$

***D_0, D_1, D_2, E_1, E_2*: Fitting parameters**

[1] K. Ito *et al.*, *J. Appl. Phys.* **128**, 095702 (2020)

Experimental results and extraction of D_{it} distribution

$$n_{\rm trap} = \int_{E_{\rm i}}^{\infty} \frac{1}{\exp\left(\frac{E - E_{\rm F}(n_{\rm free})}{k_{\rm B}T}\right) + 1} D_{\rm it}(E)\, dE$$

Extraction method

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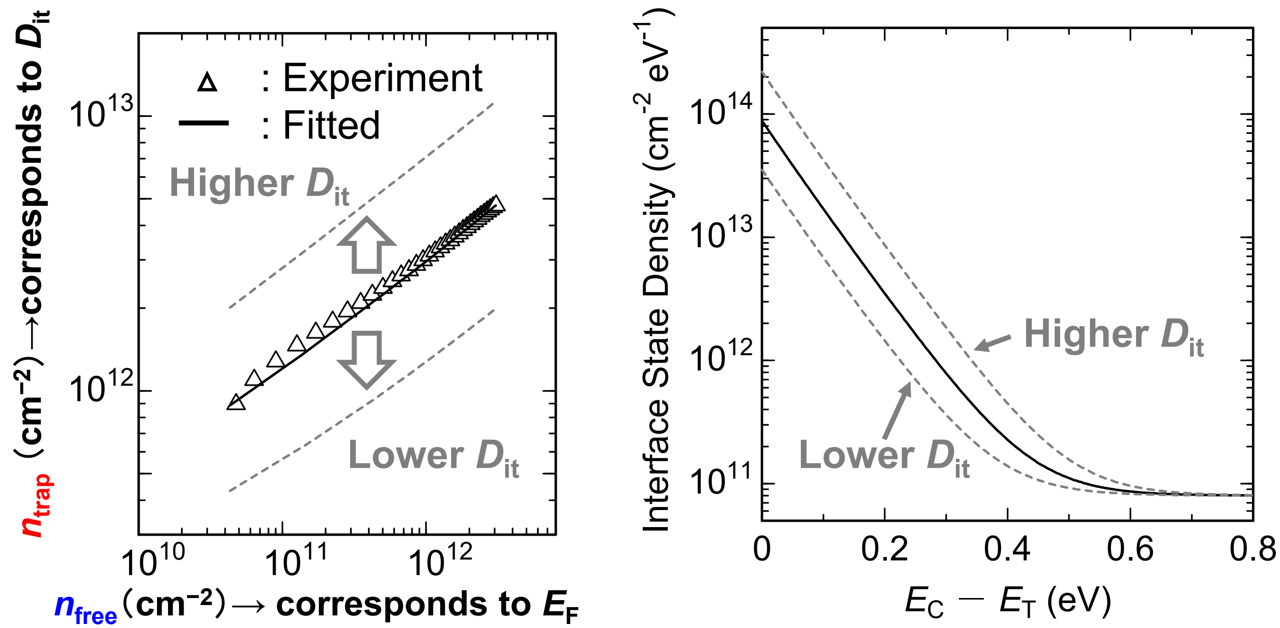
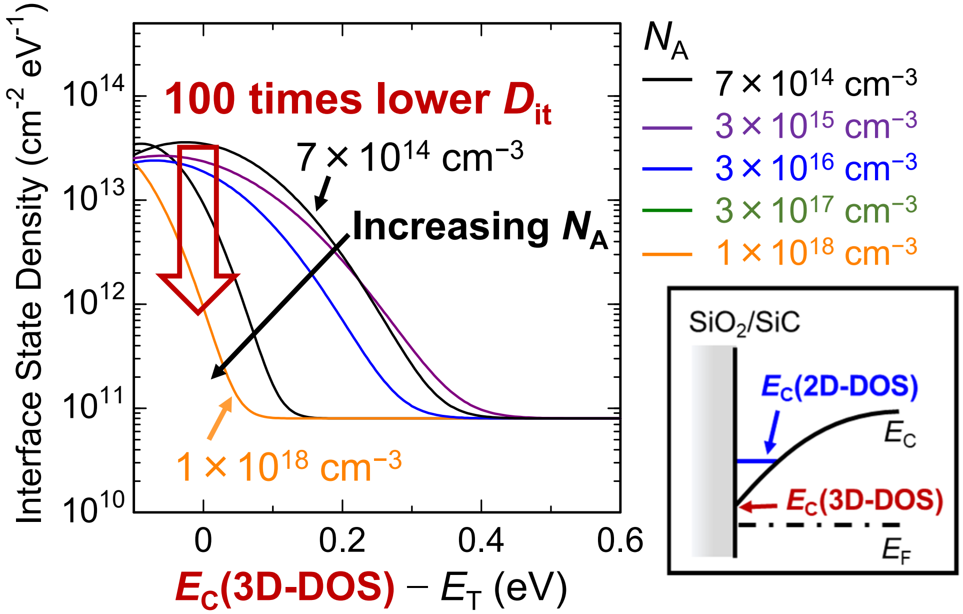


Calculate for cases where the D_{it} distribution
is **energetically fixed with respect to E_C(3D-DOS)/shifts along with E_C(2D-DOS)**

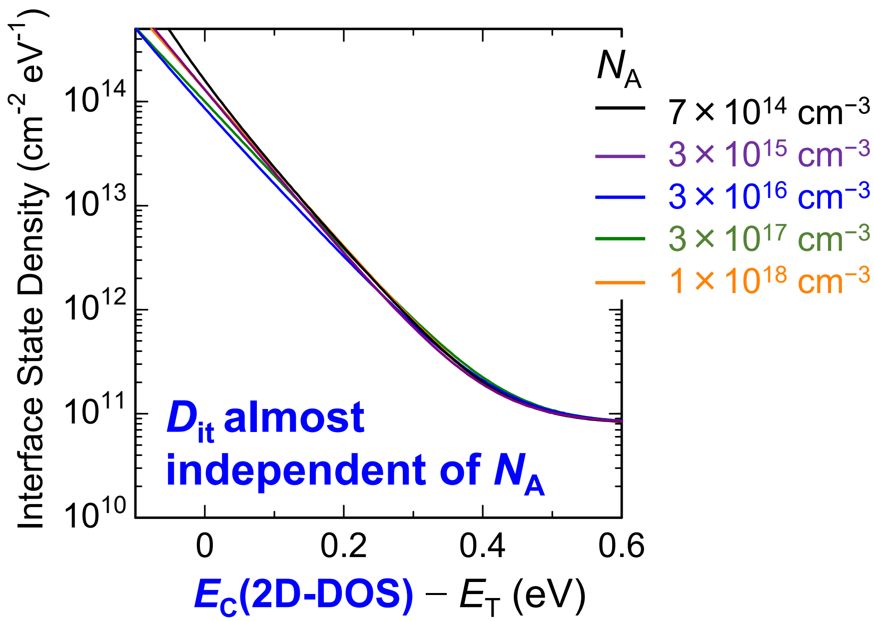
[1] K. Ito *et al.*, *J. Appl. Phys.* **128**, 095702 (2020)

D_{it} distributions extracted from n_{trap}—n_{free} characteristics

<u>D_{it} fixed with respect to E_C(3D-DOS)</u>



<u>D_{it} shifts along with E_C(2D-DOS)</u>



D_{it} values sharply decrease with N_A↑
… Hardly understandable

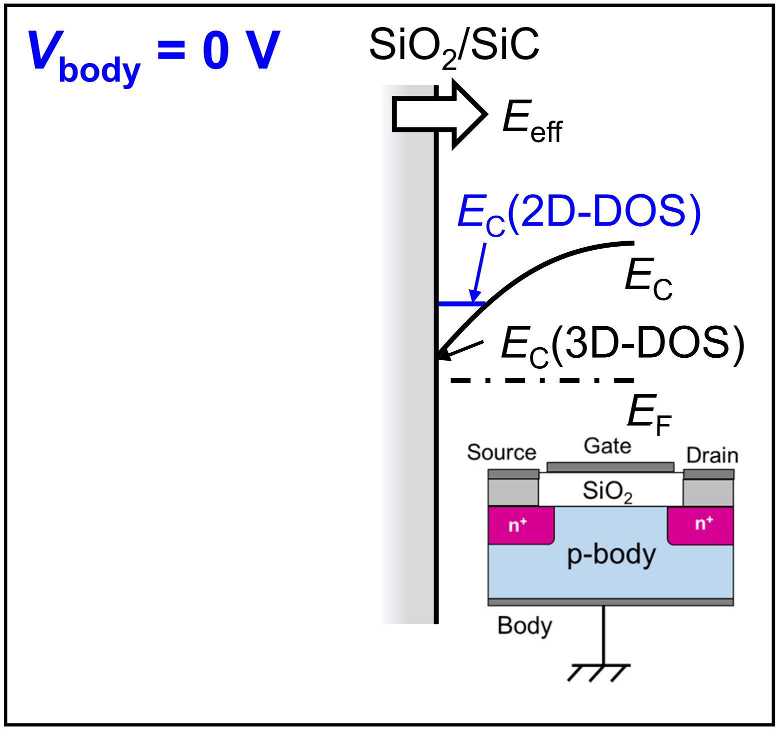
D_{it} almost independent of N_A
(determined by process) … Reasonable result

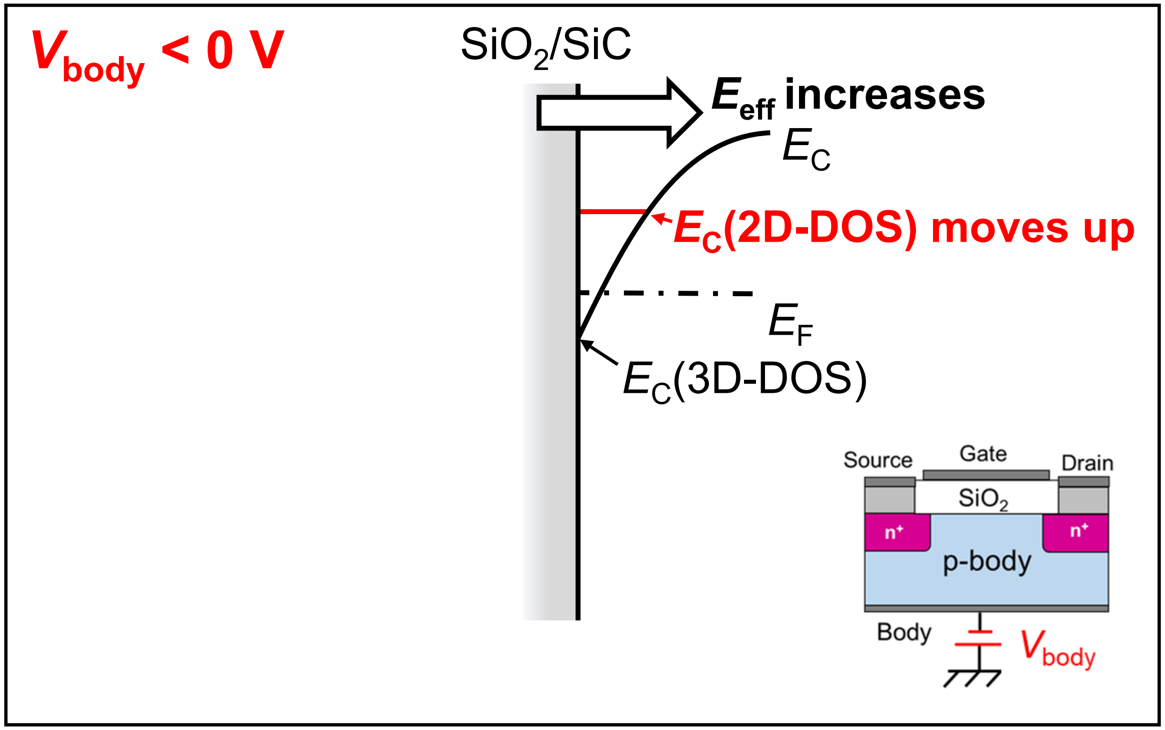
D_{it} distribution depends on N_A? … Need to verify using the same device

→ Focus on the **<u>body bias effect</u>**

Impact of body bias on n_{trap}

Negative body bias (V_{body}) : increases E_{eff}

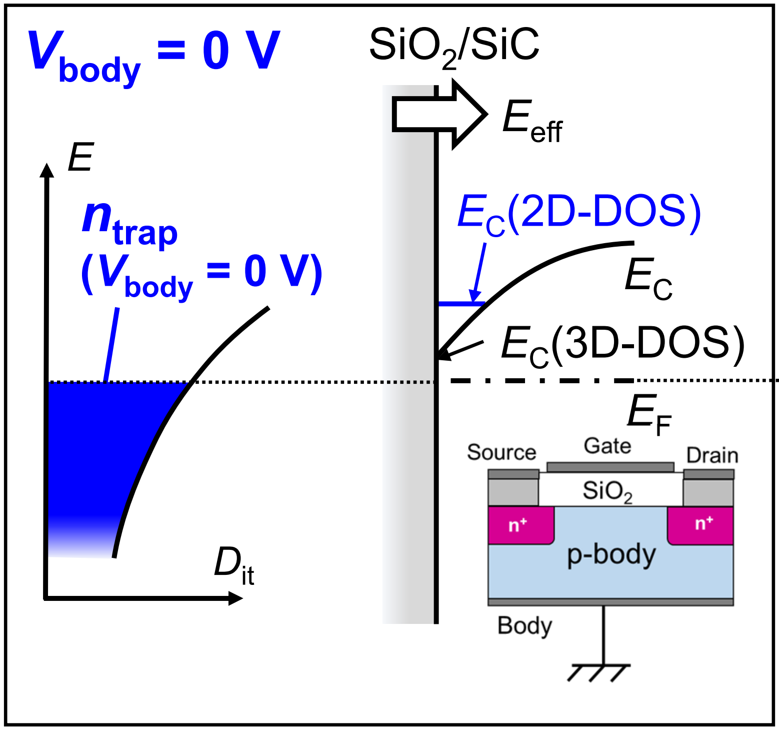


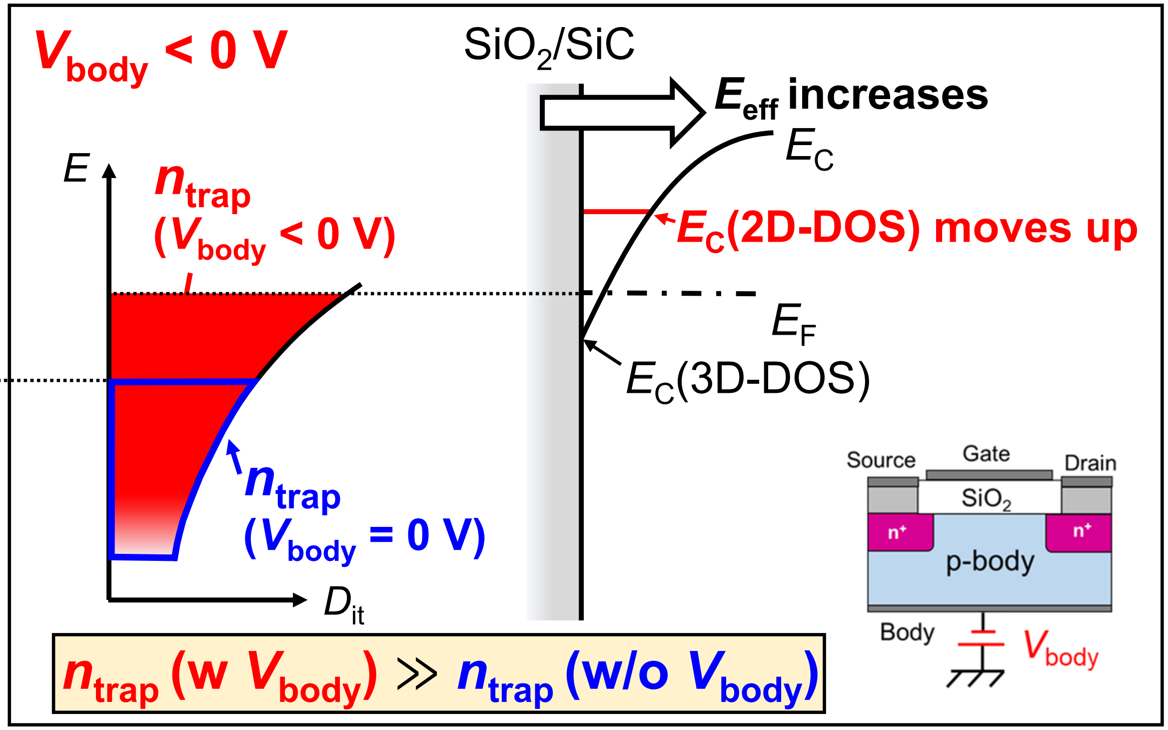


Impact of body bias on n_{trap}

Compare n_{trap} for the cases where V_{body} = 0 V and V_{body} < 0 V (@a given n_{free})

[Case 1] D_{it} distribution fixed with respect to E_C(3D-DOS)

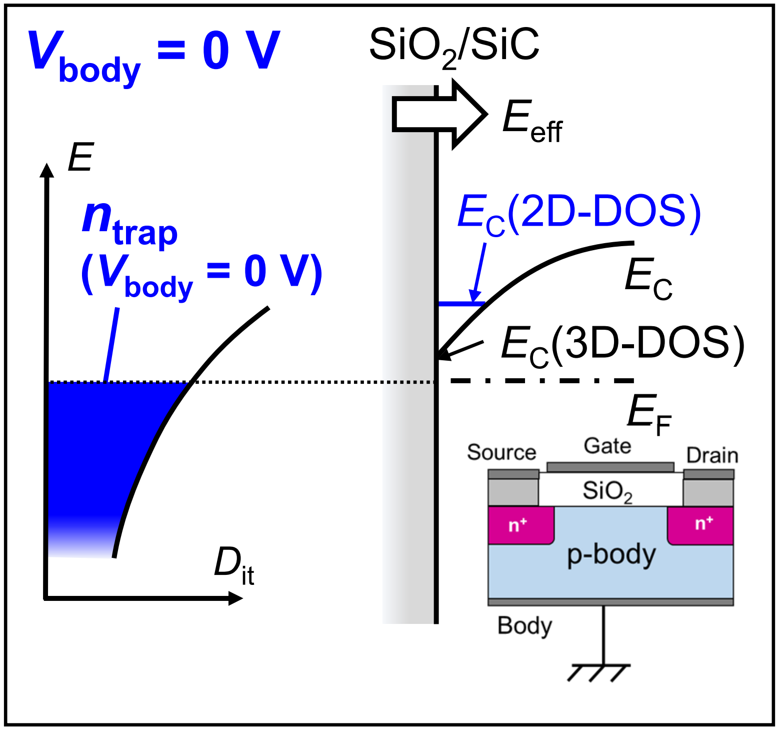


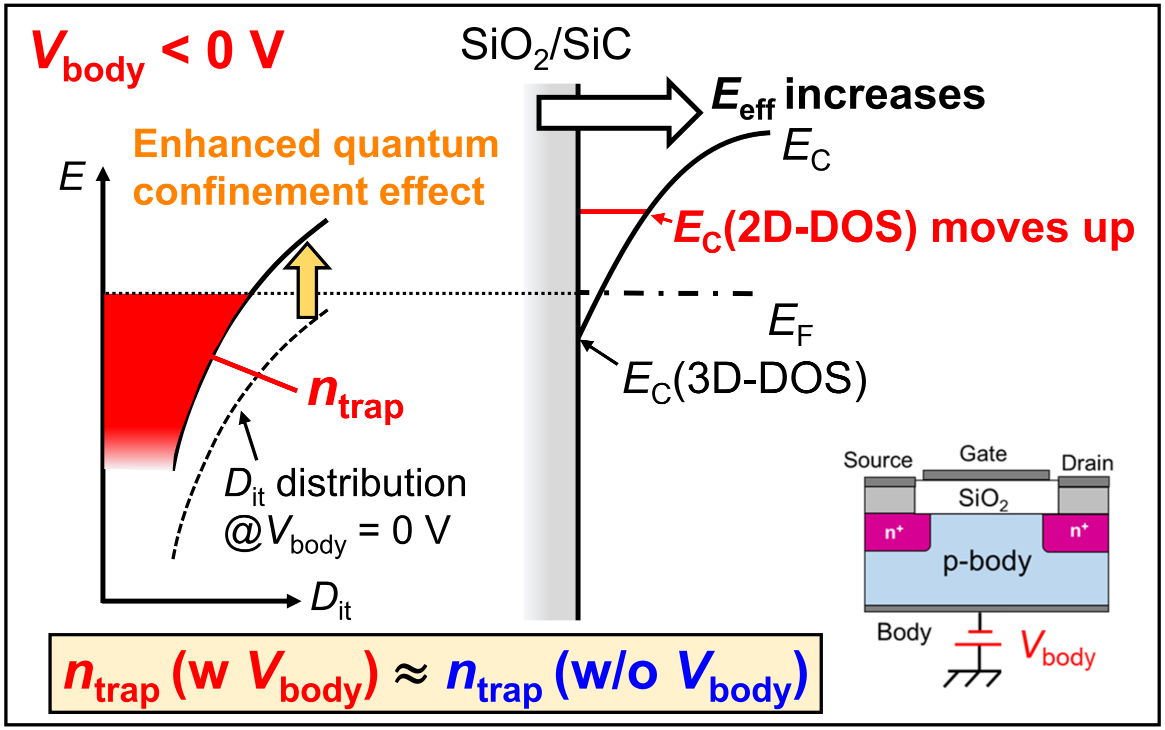


Impact of body bias on n_{trap}

Compare n_{trap} for the cases where V_{body} = 0 V and V_{body} < 0 V (@a given n_{free})

[Case 2] D_{it} distribution shifts along with E_C(2D-DOS)

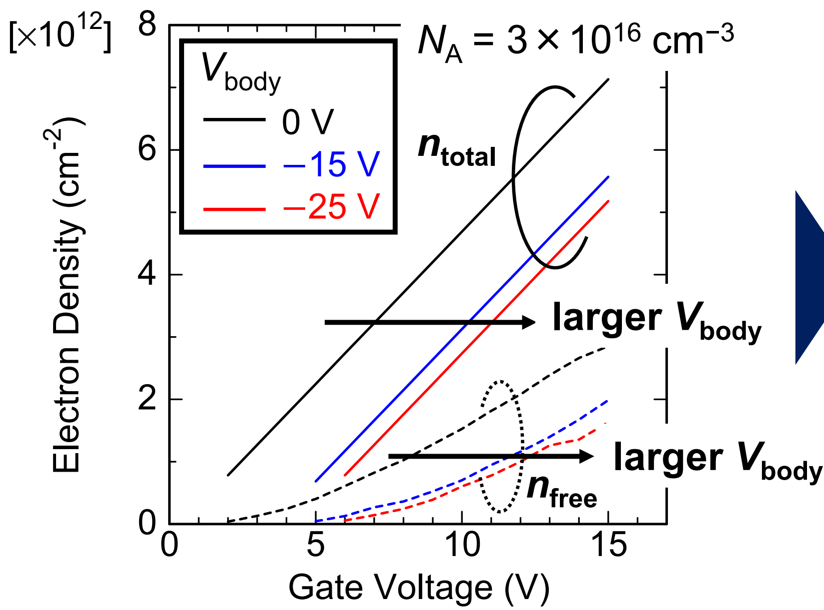




It is possible to verify whether the D_{it} distribution shifts along with E_C(2D-DOS) by **comparing n_{trap} under various V_{body}**

Body bias measurement results

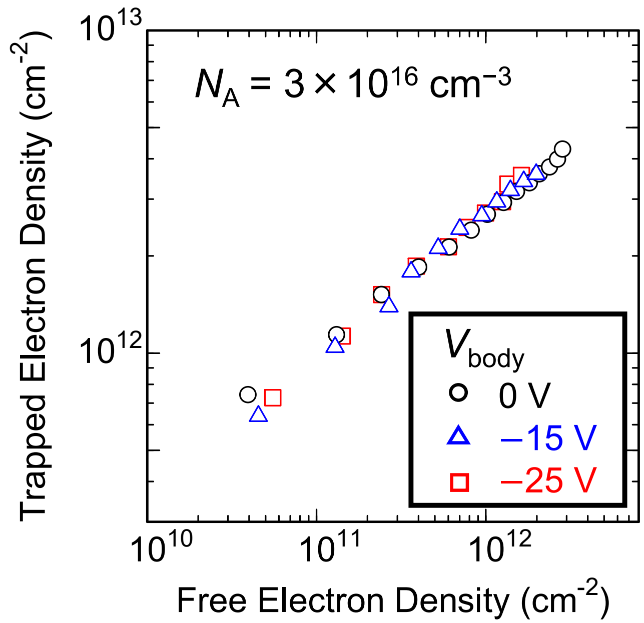
V_G dependences of electron densities



Positive shifts according to V_{body}

→ Appropriate control of V_{body}

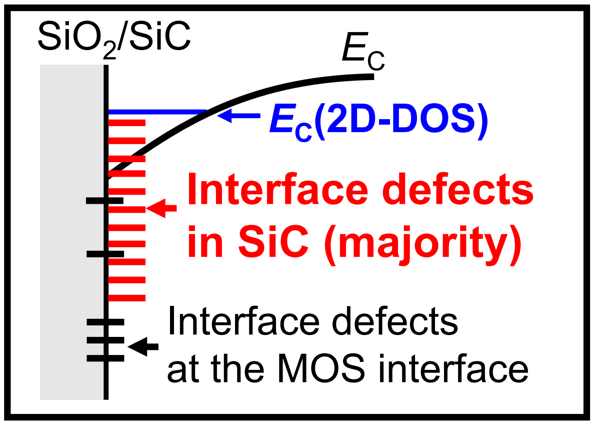
n_{trap}—n_{free} characteristics



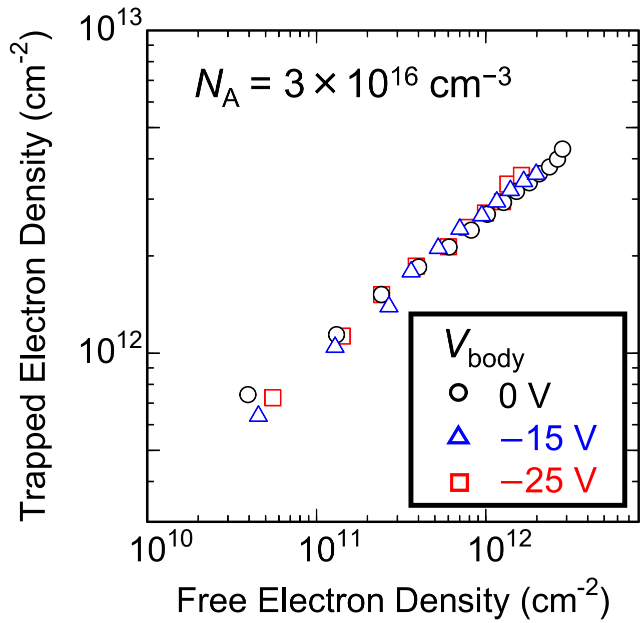
n_{trap}—n_{free} characteristics: almost independent of V_{body}

→ D_{it} distribution shifts along with E_C(2D-DOS)

Body bias measurement results



n_{trap}—n_{free} characteristics



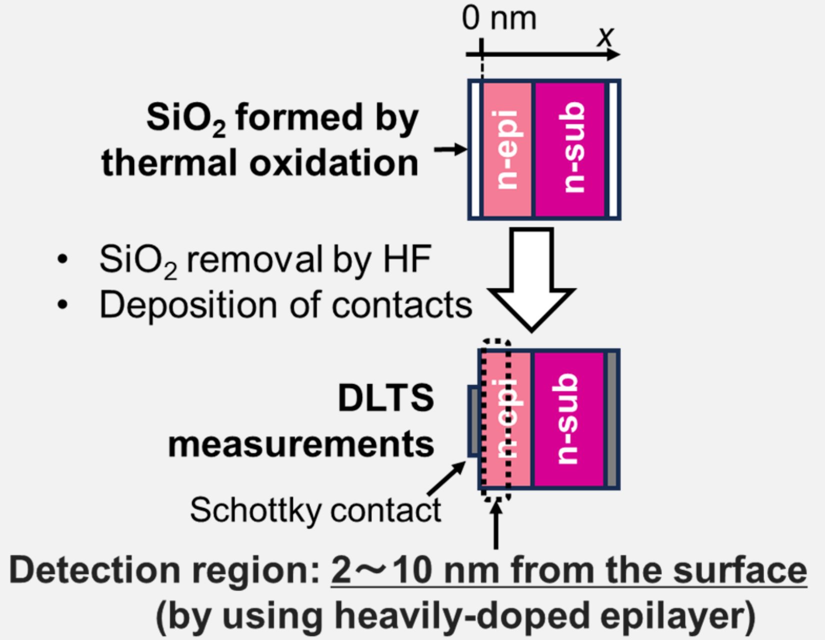
n_{trap}—n_{free} characteristics: almost independent of V_{body}

→ D_{it} distribution shifts along with E_C(2D-DOS)

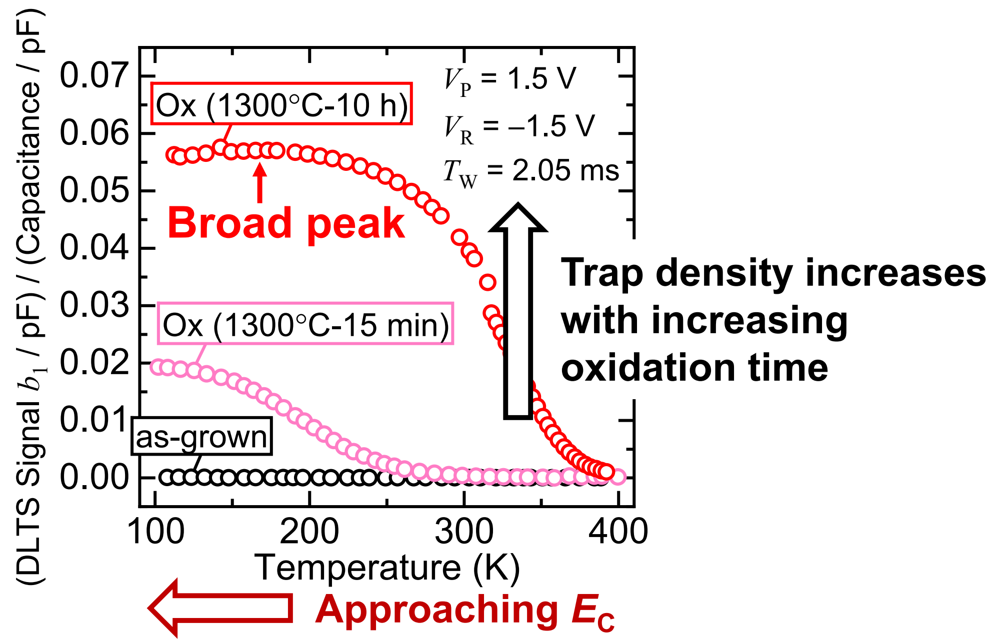
Electron trapping inside SiC

Thermal oxidation of SiC: generates multiple defect levels near E_C [1]

Sample preparation flow



DLTS spectra of fabricated samples



Defects inside SiC induced by oxidation: a primary origin of interface traps
… Electrons are trapped mainly inside SiC

[1] H. Fujii *et al., Appl. Phys. Express* **17,** 041004 (2024).

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3. Unique carrier trapping near SiC MOS interfaces

4. Carrier scattering and physics-based model of SiC MOSFETs

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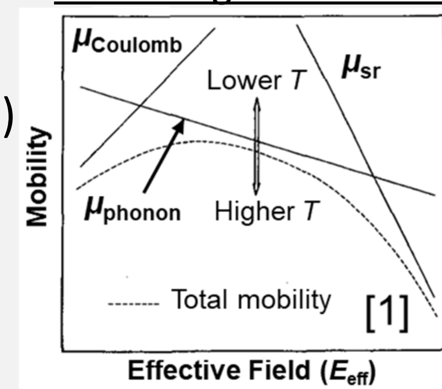
Electron scattering mechanism in MOS channels

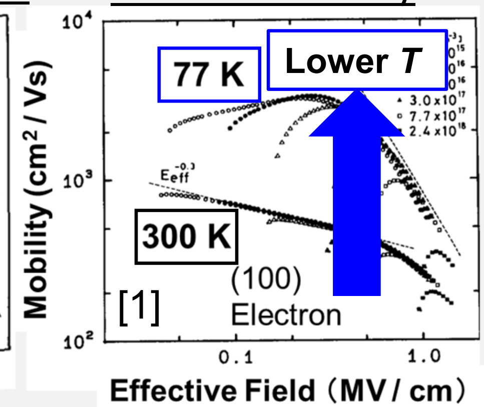
In Si MOSFETs (extremely low D_{it})

- Dominant scattering mechanism [1]
  @Low-E_{eff}: Coulomb scattering (ionized impurities)
  @Mid-E_{eff}: Phonon scattering
  @High-E_{eff}: Surface roughness (sr) scattering
- With lowering the temperature…
  $\mu_{Coulomb}$: decreases
  μ_{phonon}: increases

Scattering mechanisms



Electron mobility



[1] S. Takagi *et al., IEEE Trans. Electron Devices* **41**, 2357 (1994).

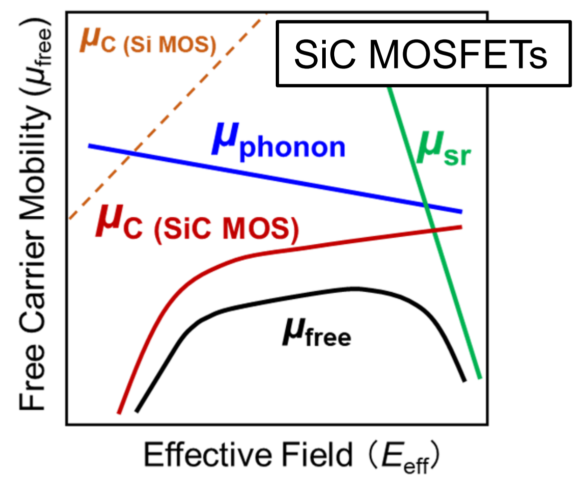
In SiC MOSFETs

High density of interface defects near the MOS interface

Coulomb scattering by non-ideal charges is dominant [2, 3]
(trapped electrons and fixed charges)

Extremely difficult to distinguish μ_{phonon} and μ_{sr}

[2] M. Noguchi *et al., Jpn. J. Appl. Phys.* **59**, 051006 (2020).
[3] K. Ito *et al., Appl. Phys. Express* **17,** 081003 (2024).

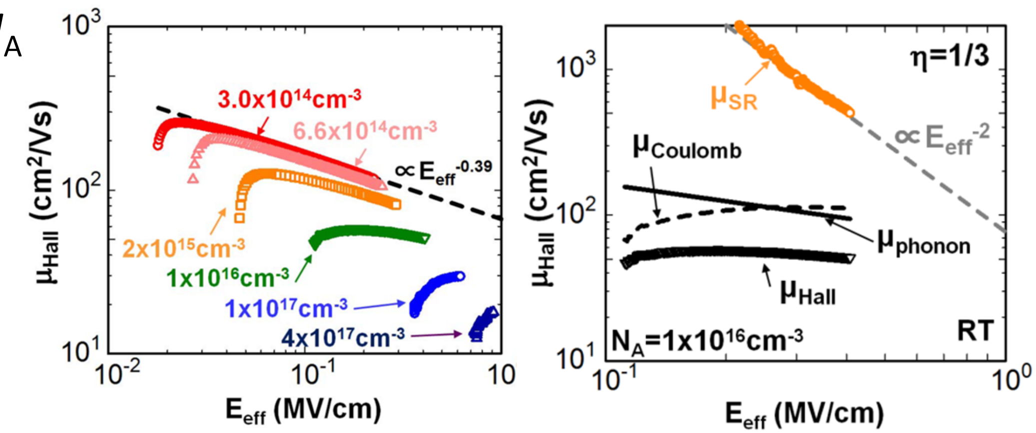


Previous report on scattering mechanism in SiC MOS channels [1]

Measurements of μ_{free} in MOSFETs with various N_A

- <u>In lightly-doped MOSFETs : $\boldsymbol{\mu_{free}} \approx \boldsymbol{\mu_{phonon}}$</u>
- Extraction of μ_{phonon}, μ_{sr}, and $\mu_{Coulomb}$ based on empirical rules

… Still lack of a physical understanding of electron scattering mechanism



[1] M. Noguchi *et al.*, *IEDM Tech. Dig.* (2017), p. 219.

Our approach

- Measure μ_{free} with varying N_A and temperature systematically
- Perform numerical calculation of μ_{free} **(considering the electron trapping inside SiC)** ← **New in this study**
- Discuss the scattering mechanism by comparing the calculated and experimental results

Calculation method of inversion layer mobility

Electronic states

Self-consistent loop

Schrödinger equation
- Subband energies
- Wavefunctions

Poisson equation
- Potential distribution

Momentum relaxation time

(next slide)

Free electron mobility
- Calculated under the relaxation time approximation

[1] H. Fujii *et al., Appl. Phys. Express* **17,** 041004 (2024).

Calculation method of inversion layer mobility

Electronic states

Self-consistent loop

Schrödinger equation

- Subband energies
- Wavefunctions

Poisson equation

- **Potential distribution**

Momentum relaxation time

(next slide)

Free electron mobility

- Calculated under the relaxation time approximation

The electron trapping inside SiC

Calculate n_{trap} with D_{it} distribution

$$n_{\mathrm{trap}} = \int_{E_{\mathrm{i}}}^{\infty} f(E)\, \boldsymbol{D}_{\mathbf{it}}(\boldsymbol{E})\, dE$$

$D_{it}(E)$: **shifts along with E_C(2D-DOS)**

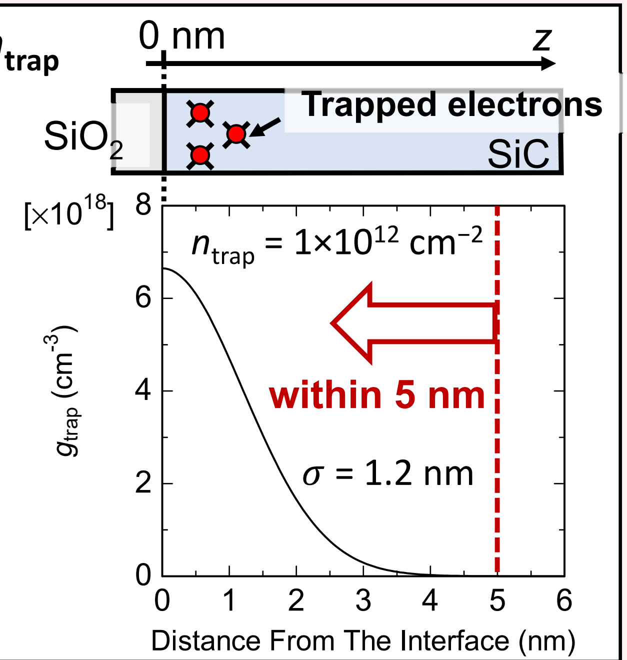
Calculate the distribution of n_{trap}

Depth profile of n_{trap} :

$$g_{\mathrm{trap}}(z) = \frac{2n_{\mathrm{trap}}}{\sqrt{2\pi\boldsymbol{\sigma}^2}} \exp\left(-\frac{z^2}{2\boldsymbol{\sigma}^2}\right)$$

(**half Gaussian function** [1])

Trapped electrons:
Distributed **within 5 nm** from the MOS interface



[1] H. Fujii *et al., Appl. Phys. Express* **17,** 041004 (2024).

Scattering mechanism

Phonon scattering

- Acoustic phonon（ac）& Non-polar optical phonon（nop）scatterings [1]
- Parameters: **deformation potential（D_{ac}, D_{nop}）**
  (Adjusted from the bulk deformation potentials $D_{ac, bulk}$ and $D_{nop, bulk}$ [2])

Surface roughness (sr) scattering

- Correlation function: $\langle \Delta(r_0)\Delta(r_0 + r)\rangle = \Delta_{sr}^2 e^{-\sqrt{2}|r|/L_{sr}}$ (common to Si MOS) [1]
- Parameters: **height（Δ_{sr}）** and **correlation length（L_{sr}）of surface roughness**

Common to Si MOS

Coulomb scattering by non-ideal charges (peculiar to SiC MOS)

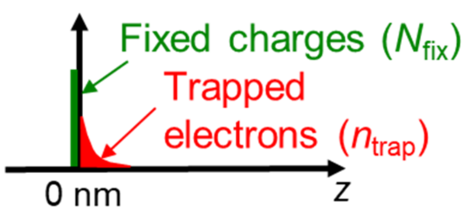
Fixed charges (N_{fix})

- Locates at the MOS interface
- **N_{fix} value: fitting parameter**

Trapped electrons (n_{trap})

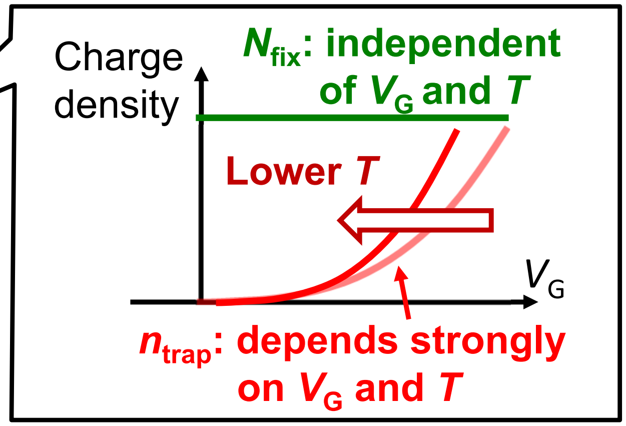
- n_{trap}: calculated with D_{it} distribution
- Distributes inside SiC
  （**σ: fitting parameter**）

Charge distributions



Depth profile of n_{trap}:

$$g_{trap}(z) = \frac{2n_{trap}}{\sqrt{2\pi\sigma^2}}\exp\left(-\frac{z^2}{2\sigma^2}\right)$$



[1] H. Tanaka and N. Mori, *Jpn. J. Appl. Phys.* **59**, 031006 (2020). [2] H. Iwata and K. M. Itoh, *J. Appl. Phys.* **89**, 6228 (2001).

Scattering mechanism

Phonon scatterin

- Acoustic phon
- Parameters: de

(A

Surface roughne

- Correlation fu
- Parameters: he

Coulomb scatter

Fixed charges (N_{fi}

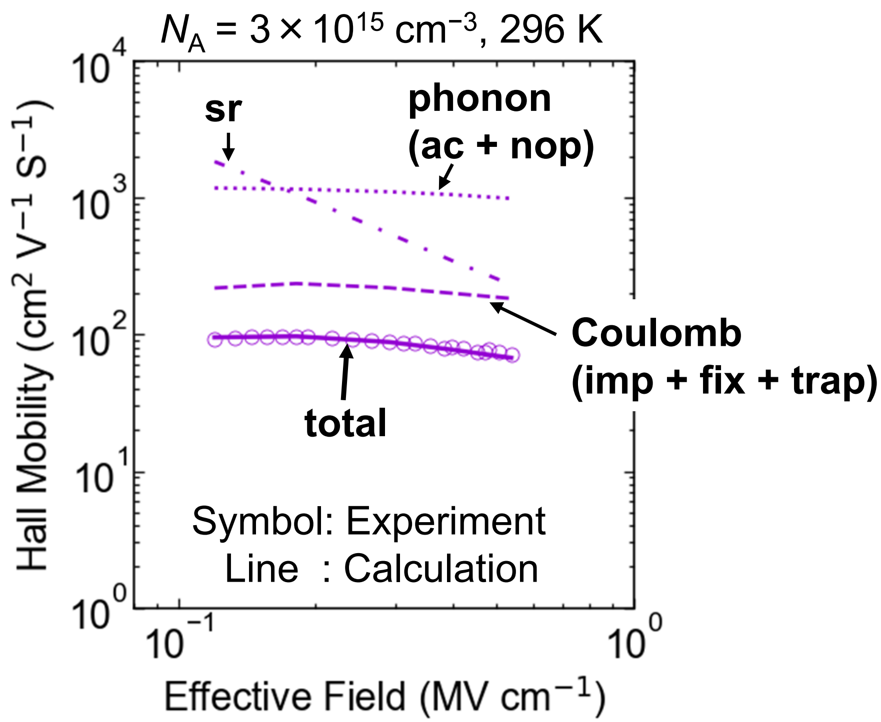
- Locates at the
- N_{fix} value: fitti

Trapped electron

- n_{trap}: calculate
- Distributes ins

(σ: fitting par

Example of calculated results



Parameters are uniquely determined by simultaneously reproducing experimental μ_{Hall} at different temperatures

Common to Si MOS

: independent of V_G and T

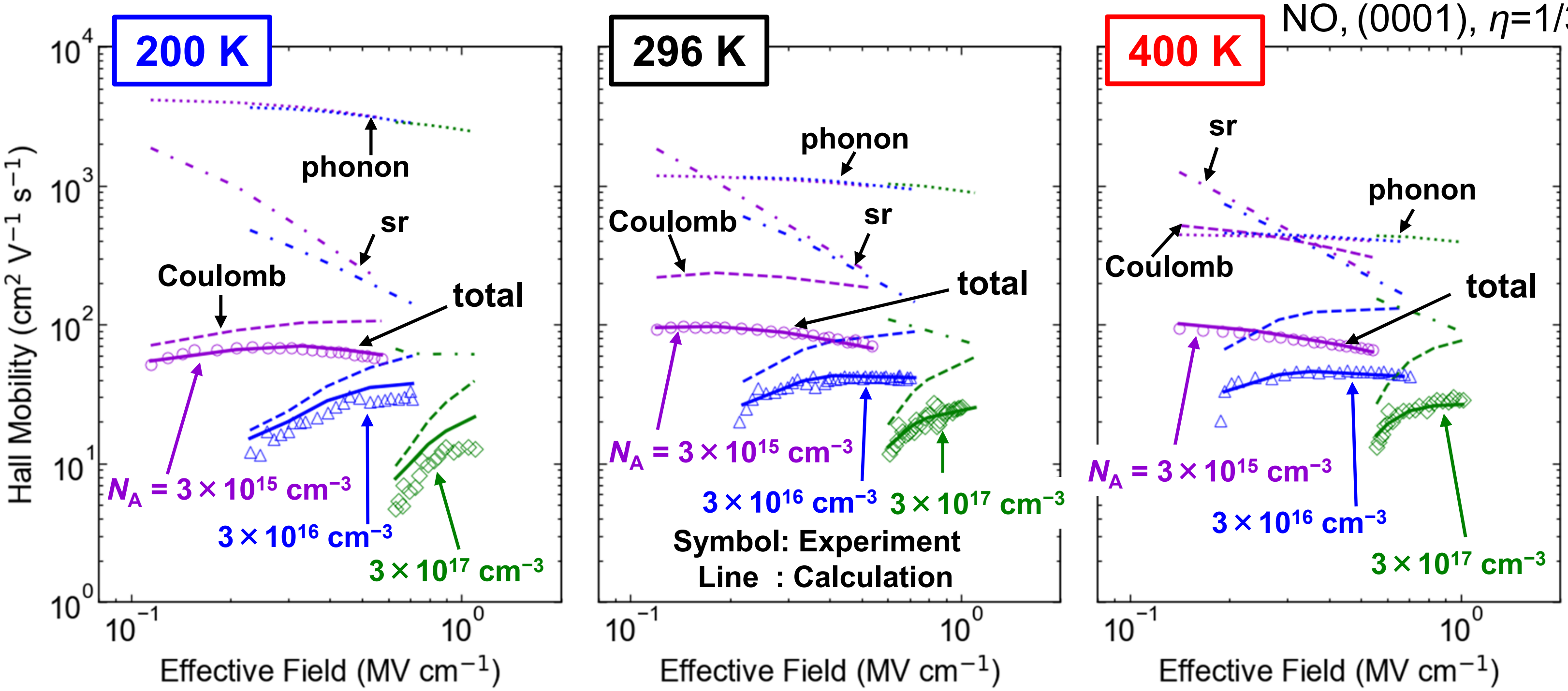
er T

V_G

ends strongly V_G and T

[1] H. Tanaka and N. Mori, *Jpn. J. Appl. Phys.* **59**, 031006 (2020). [2] H. Iwata and K. M. Itoh, *J. Appl. Phys.* **89**, 6228 (2001).

Experimental and calculated μ_{free}



Phonon scattering

D_{ac} = 0.85$D_{ac,\ bulk}$ [1]

D_{nop} = 0.85$D_{nop,\ bulk}$ [1]

Surface roughness scattering

Δ_{sr} = 1 nm L_{sr} = 5 nm

Coulomb scattering

σ = 1.2 nm

N_{fix} (cm^{-2}) :

4.8×10^{12} (N_A = 3×10^{15} cm^{-3})

1.4×10^{13} (N_A = 3×10^{16} cm^{-3})

1.8×10^{13} (N_A = 3×10^{17} cm^{-3})

All parameters: independent of *T*

Reproducing experimental μ_{Hall} in a wide range of E_{eff} and *T* with reasonable parameters

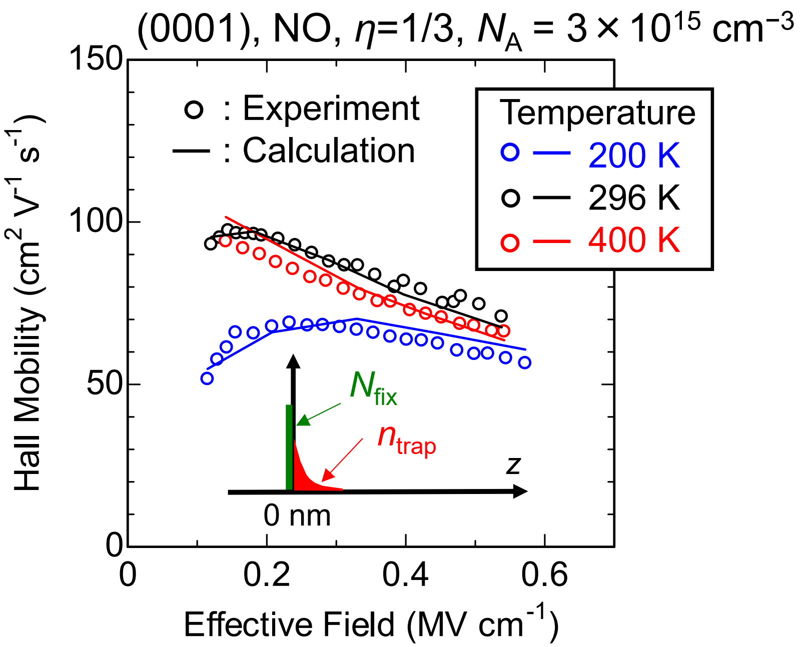
→ Elucidation of the electron scattering mechanism in SiC MOS channels

[1] H. Iwata and K. M. Itoh, *J. Appl. Phys.* **89**, 6228 (2001).

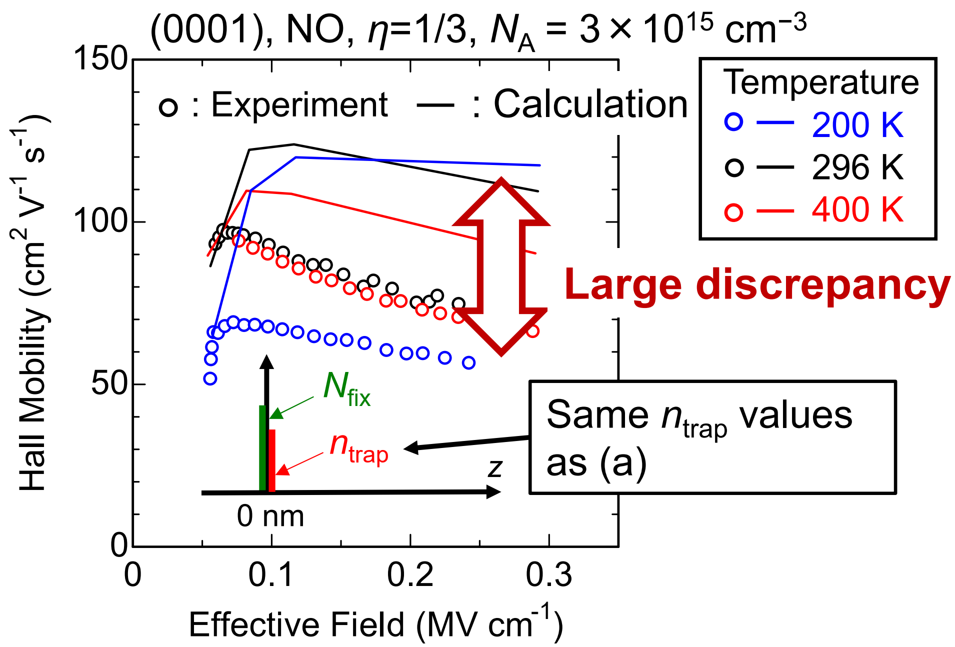
Validation of electron trapping inside SiC

Calculations consider trapped electrons <u>only at the MOS interface</u> were also performed

<u>(a) n_{trap} distributed in SiC</u>



<u>(b) n_{trap} at the interface</u>



Calculated results for case (b): much different from the experimental results
→ Trapped electrons are actually distributed inside SiC

Calculation of gate characteristics

Drain current

$$I_D = e n_{free} \boldsymbol{\mu_{free}} V_D$$

Calculated by the proposed model

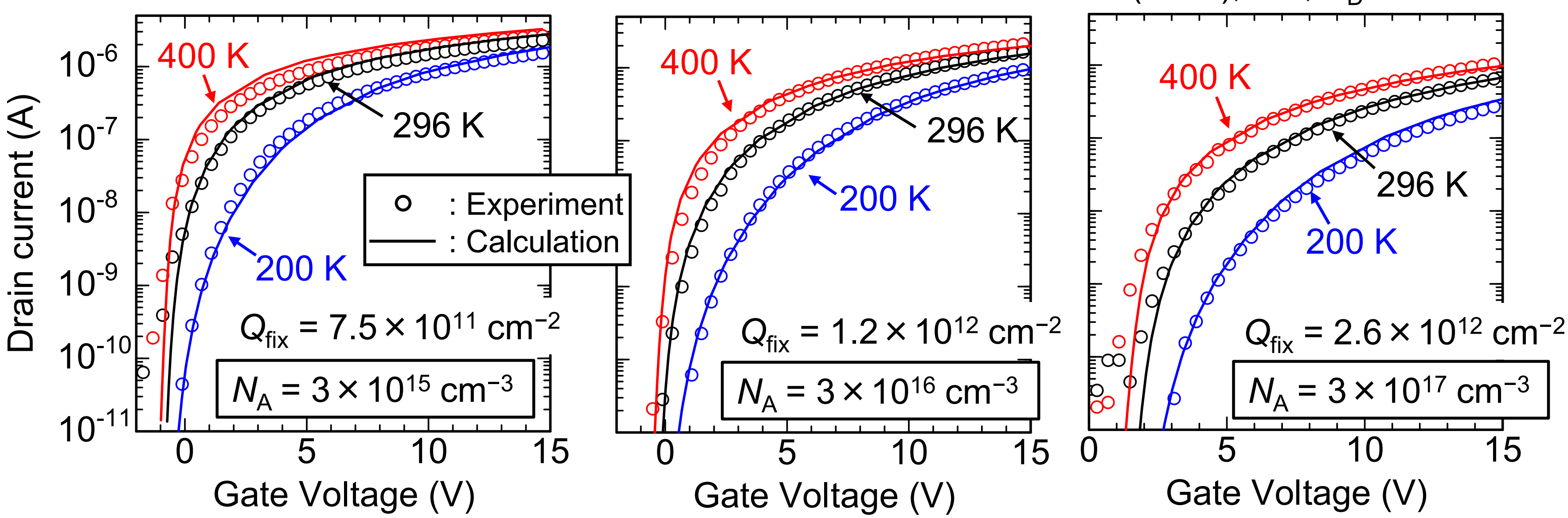
Gate voltage

$$V_G = \psi_{ms} + \psi_s + \frac{e(-\boldsymbol{Q_{fix}} + N_A z_{depl} + n_{free} + \boldsymbol{n_{trap}})}{C_{ox}}$$

Fitting parameter ... Independent of V_G and T

Calculated with D_{it} distribution ... Same D_{it} distribution for all devices

(0001), NO, V_D = 0.1 V



Good agreement with experimental results in a wide I_D range from 10^{-10} to 10^{-6} A

Outline of this talk

1. Background and purpose of this study

2. Device fabrication and measurements

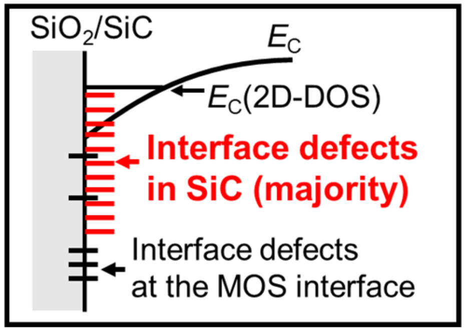
3. Unique carrier trapping near SiC MOS interfaces

4. Carrier scattering and physics-based model of SiC MOSFETs

5. Summary

Summary

Modeling of SiC MOSFETs based on a physical understanding of electron trapping and scattering mechanisms in SiC MOS channels



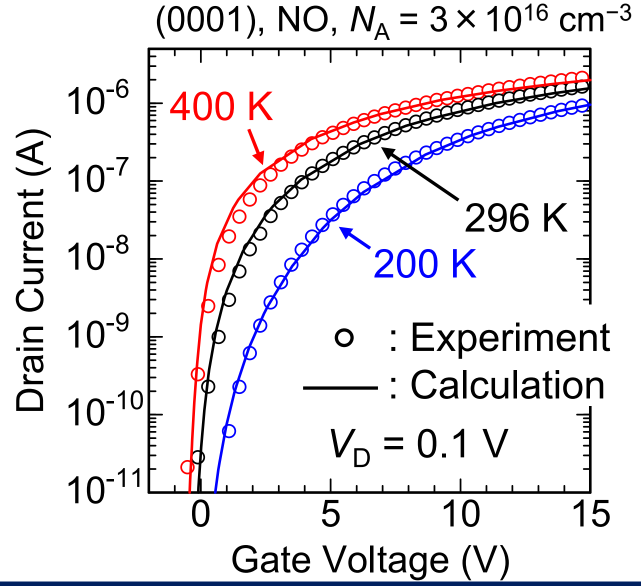
□ Unique carrier trapping near SiC MOS interfaces

- D_{it} distribution in SiC MOS shifts along with E_C(2D-DOS)
  → Most of the interface traps are located inside SiC
  （Electrons are trapped mainly inside SiC）

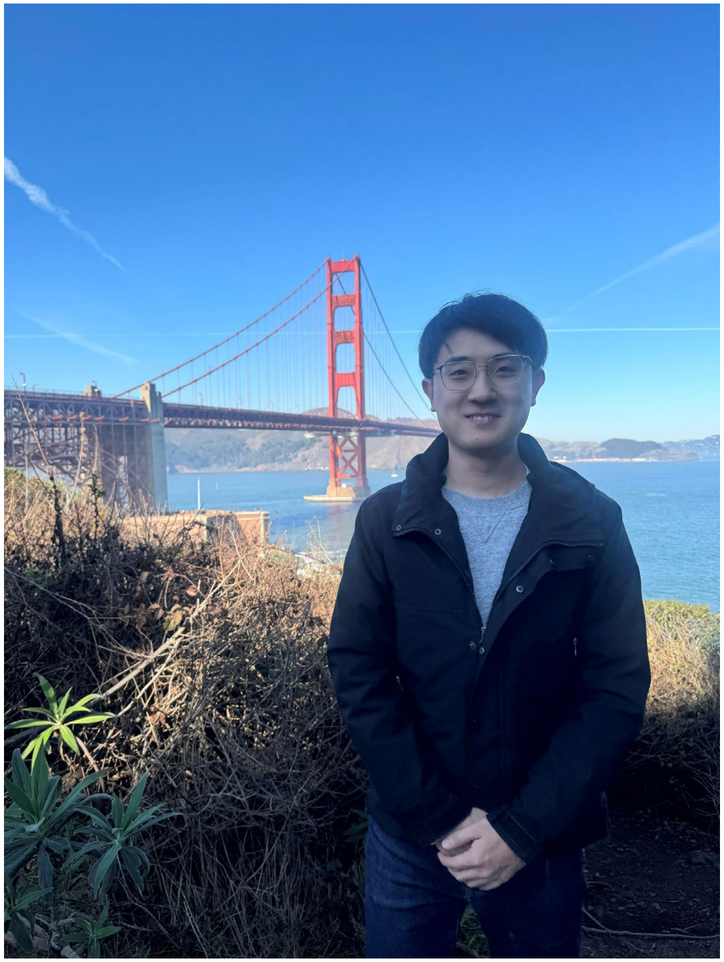
□ Carrier scattering and physics-based model of SiC MOSFETs

- Calculations that take into account the electron trapping inside SiC
  → Successfully reproduced μ_{Hall} and gate characteristics in the temperature range of 200 ～ 400 K

First physics-based model for SiC MOSFETs



Self Introduction



Xilun Chi

Kyoto University, Dept. of Electronic Sci. & Eng.

- **Degree**: third-year Ph.D. student
- **Undergraduate Studies**: Electrical and Electronic Engineering
- **Research Topic**: Carrier Scattering and Mobility Modeling in SiC MOS Channels
- **Awards**: IEEE EDS Japan Joint Chapter Student Award (Feb. 2025)
- **Publications**: 2 papers (IEDM Tech. Digest, JJAP)
- **Presentations**: 3 times at ICSCRM (2 oral, 1 poster), 1 time at IEDM (oral)