Introduction of SiC Power Device Reliability Lab

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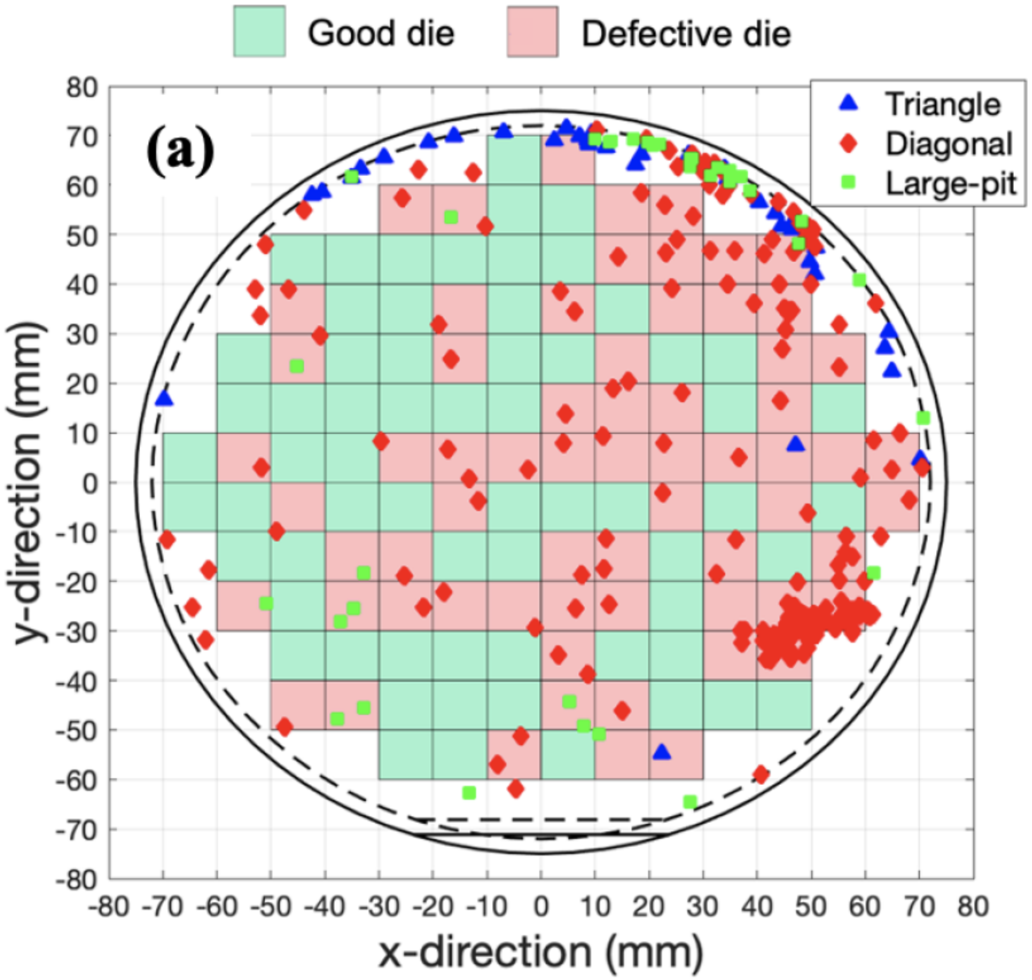
The Ohio State University

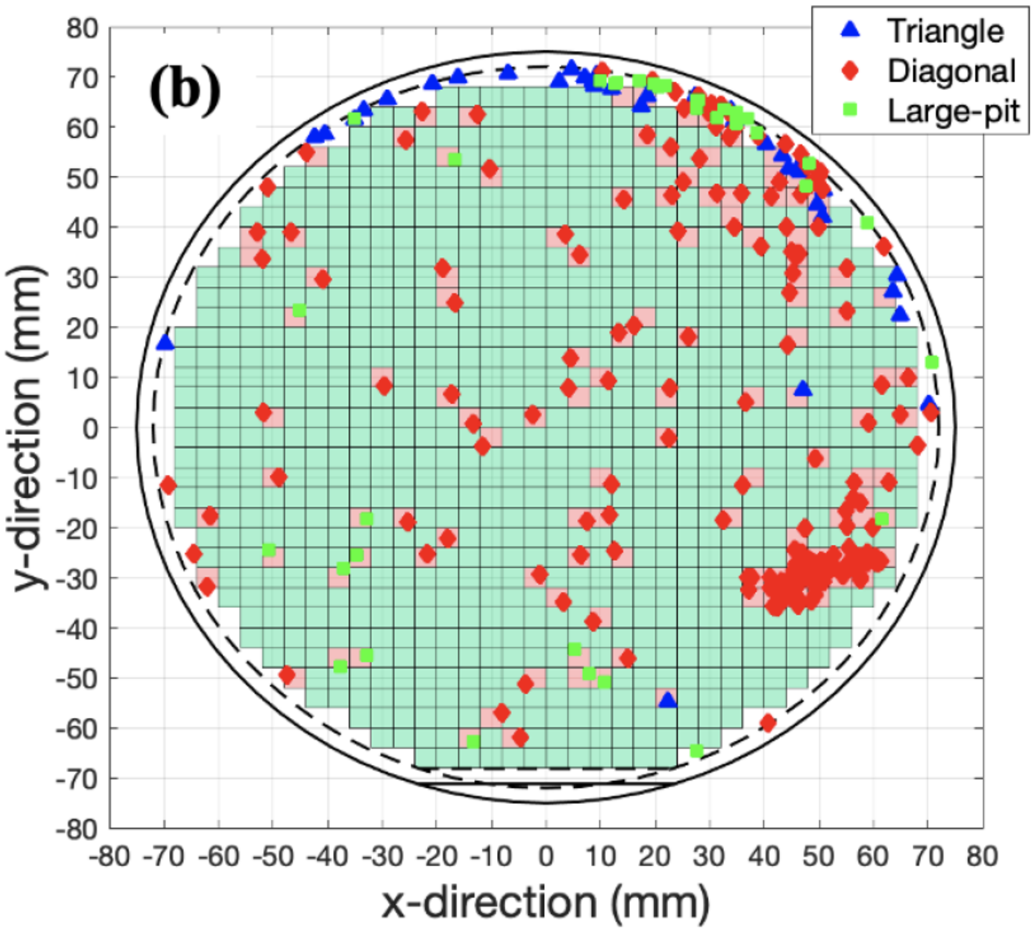
Current Challenges in SiC Technology

Higher Gate Oxidation Defects	→	Early GOX Breakdown
Basal Plane Dislocation	→	Body Diode Degradation
Defects in Bulk or Poor JFET and Termination Design	→	Early Drain-Source Failure
Shorter Short Circuit Withstand Time	→	Weaker Short Circuit Ruggedness

Area Dependent Defects on Yield in SiC Wafer



Wafer map with die area 10mmx10mm having 49% yield



Wafer map with die area 4mm x 4mm having 87% yield

PhD Students Supported by II-VI Coherent Block Gift Program

Name	Graduated In	Current Status
Susana Yu	2022 (PhD)	Employed at SemiQ, USA
Shengnan Zhu	2023 (PhD)	Employed at Ford Motor Company, USA
Limeng Shi	2024 (PhD)	Employed at SemiQ, USA
Monikuntala Bhattacharya	Expected to graduate Aug, 2025 (PhD)	Placed at L&T Semiconductor Technologies Limited, India
Shiva Houshmand	Expected to graduate Aug, 2025 (MS)	

SiC Power MOSFET Reliability with Device Design Insight

Monikuntala Bhattacharya

Advisor: Prof. Anant K. Agarwal

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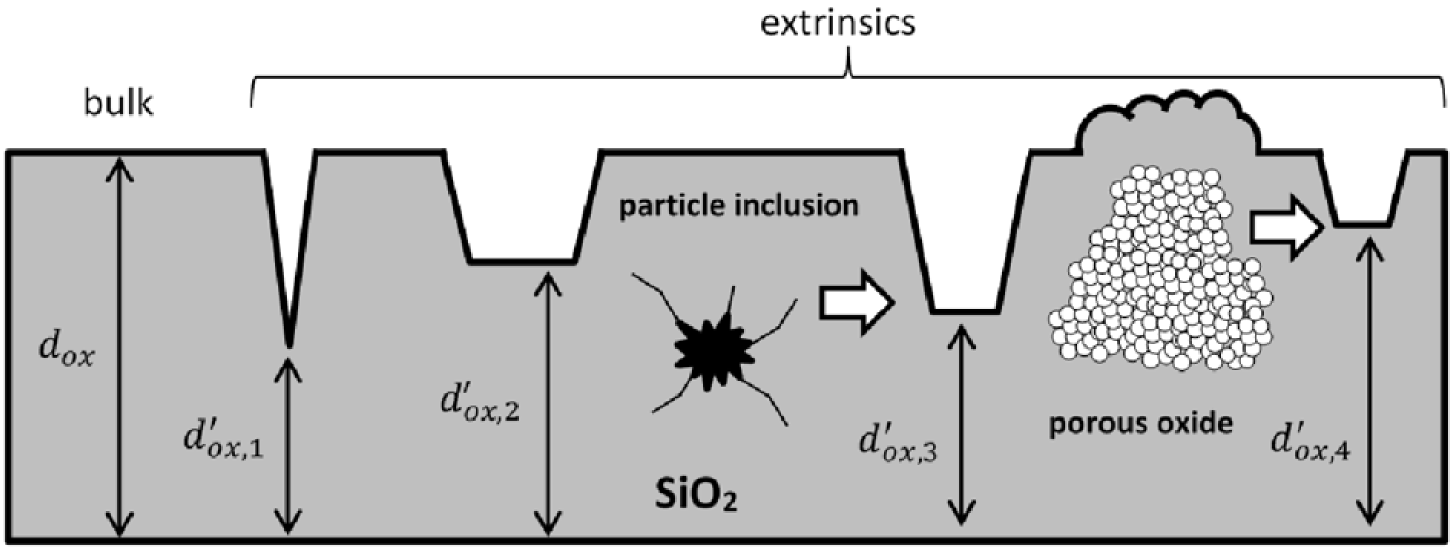
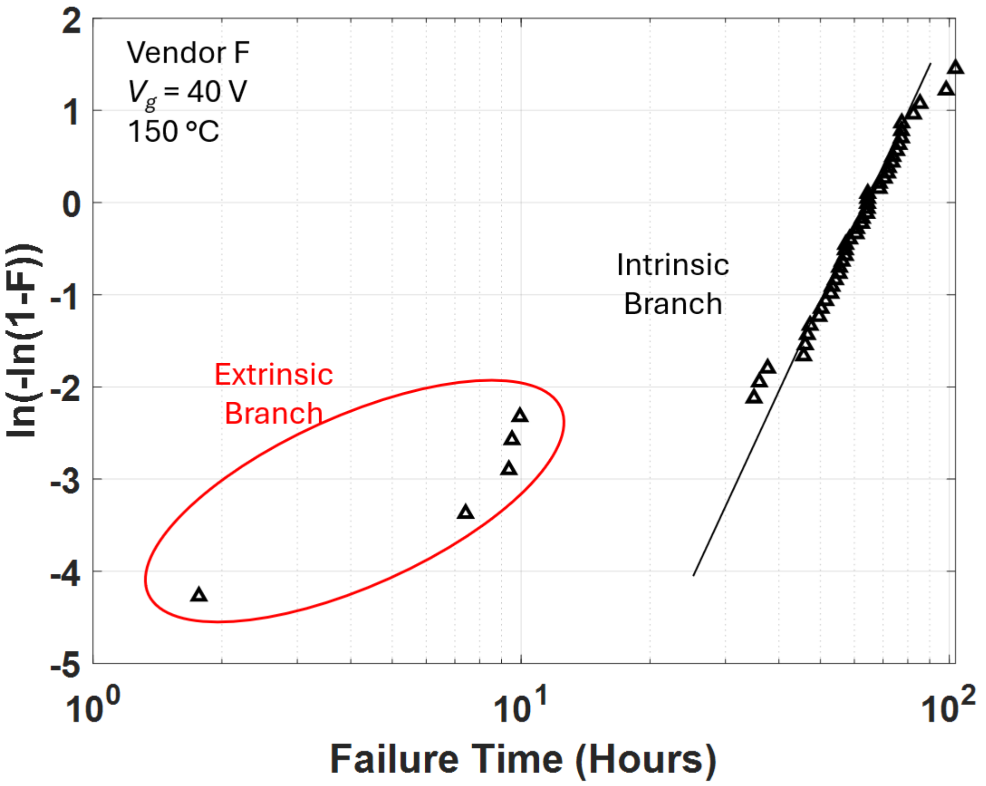
Topics

<u>1. Analysis of Gate Oxide Screening Techniques</u>

2. Development of 3.3 kV SiC Power MOSFETs

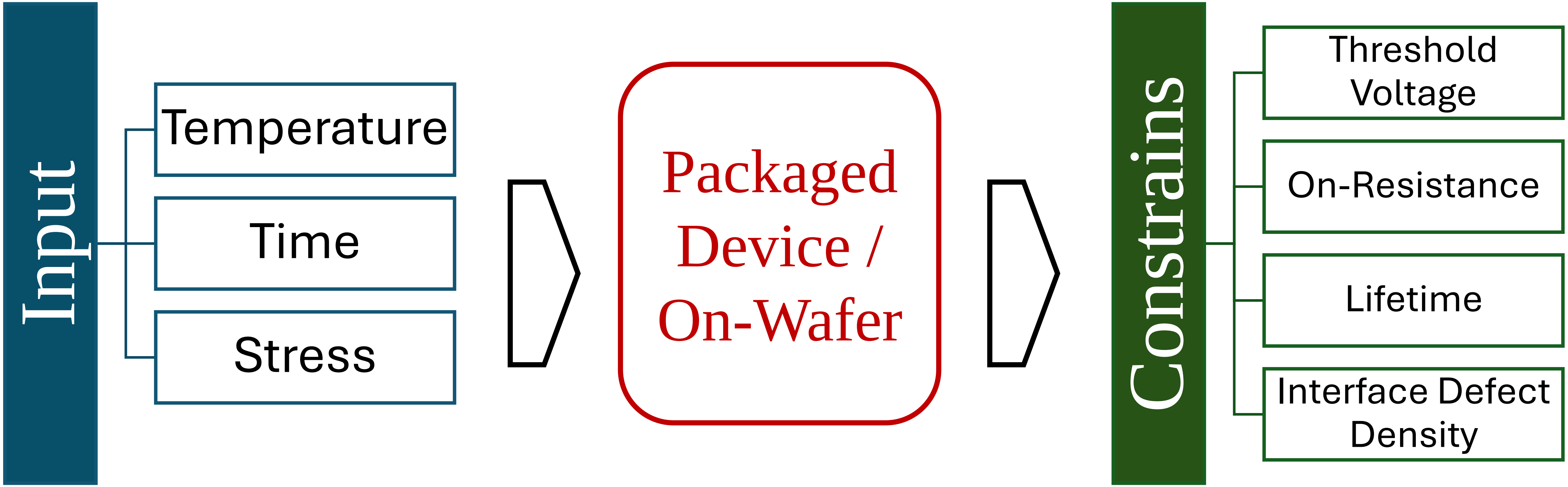
Origin of Early Failures : Oxide Thinning Model





[1] T. Aichinger and M. Schmidt, "Gate-oxide reliability and failure-rate reduction of industrial SiC MOSFETs", *2020 IEEE International Reliability Physics Symposium (IRPS)*, pp. 1-6, 2020.

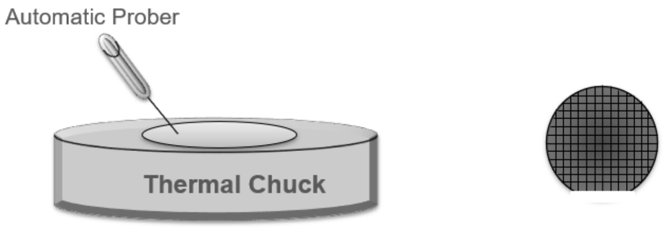
Overview of Gox Screening



Gox Screening Techniques

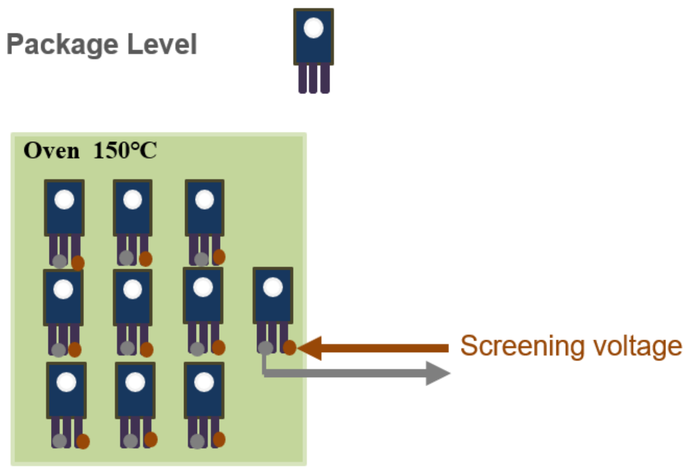
Wafer Level Gate Oxide Screening

- **Conventional Gate Oxide Screening**
- **Screening With Adjustment Pulse**

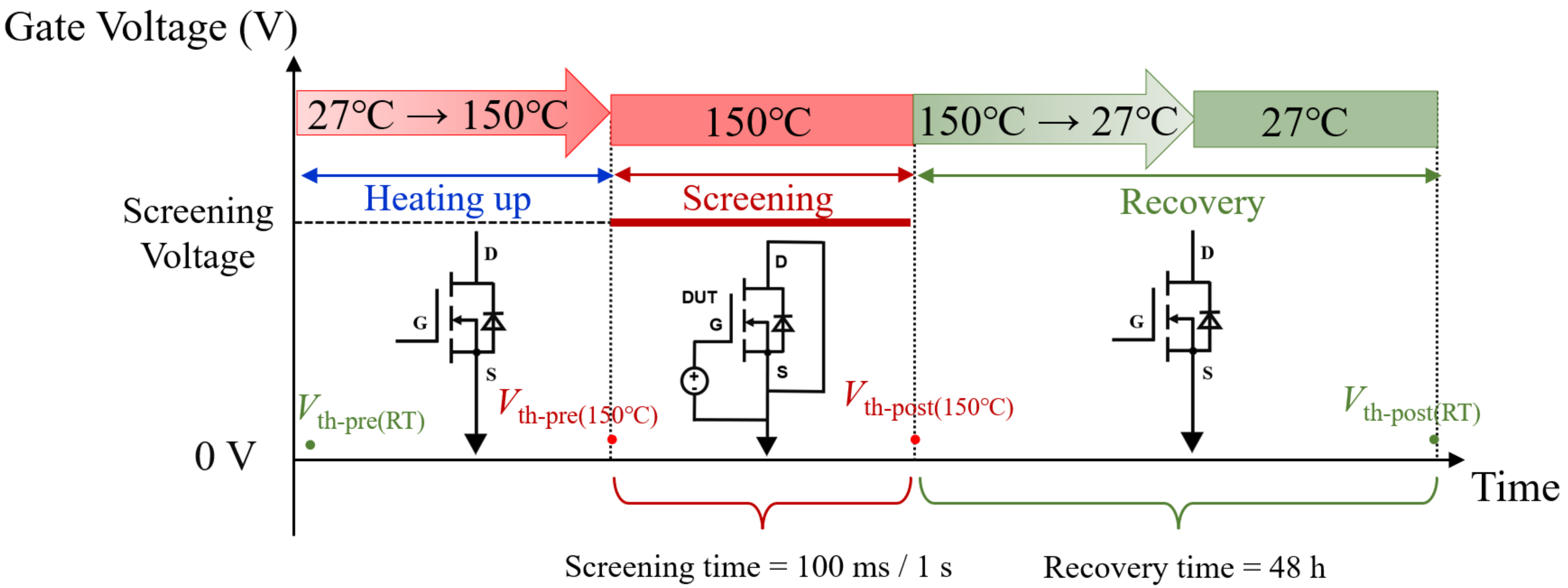


Burn-in

- **DC Burn-in**
- **Pulsed Voltage Burn-in**



Conventional Gox Screening



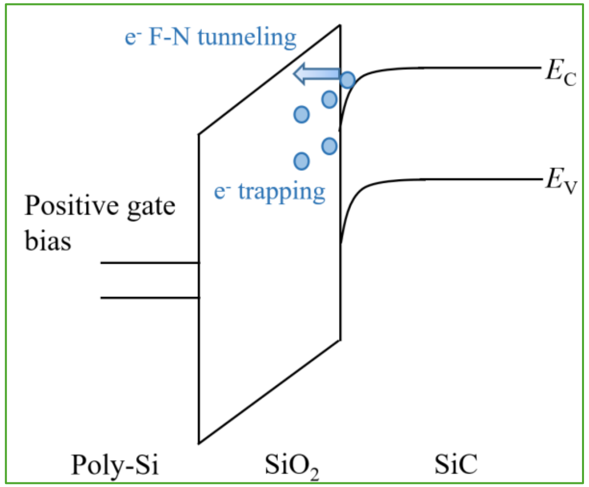
$$\Delta V_{th} = V_{th,post} - V_{th,pre}$$

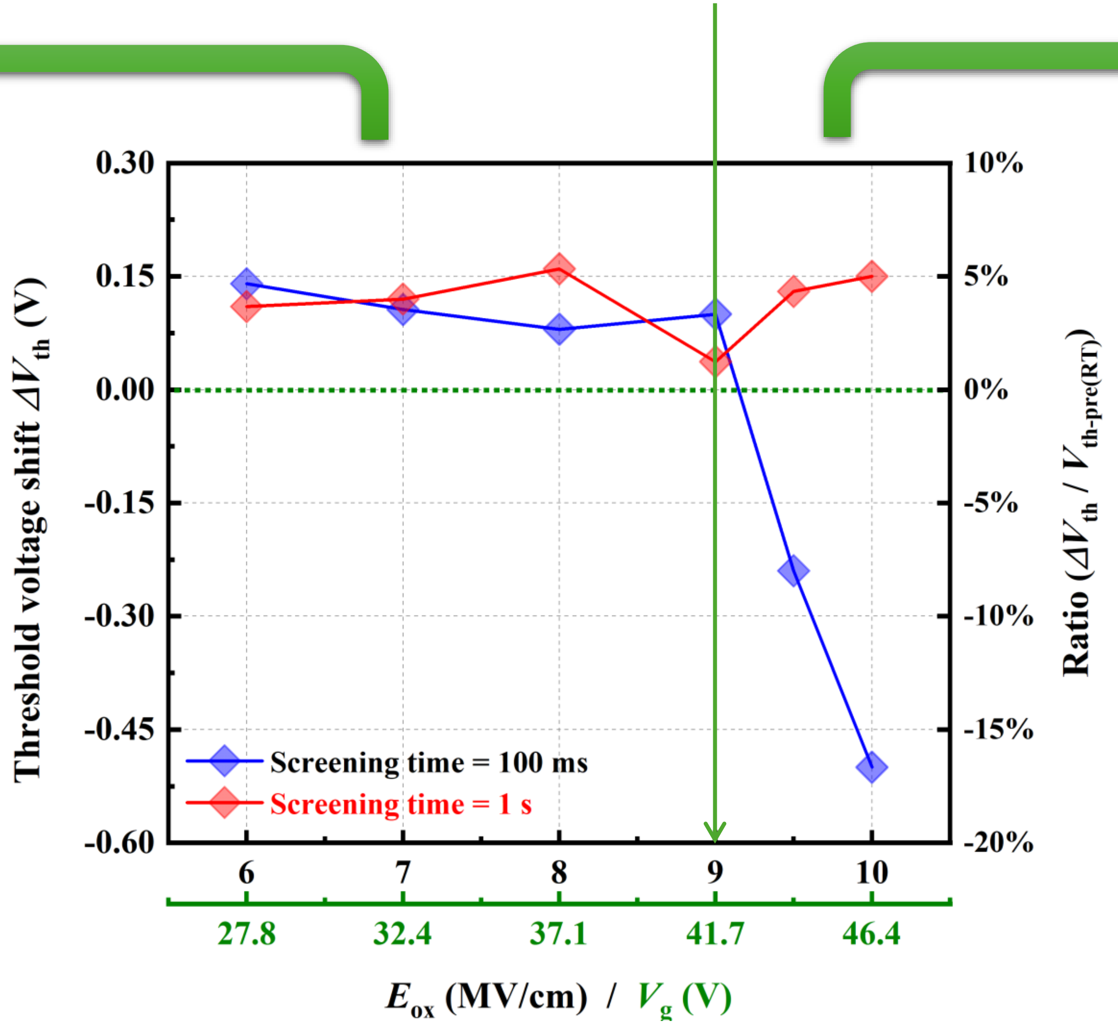
$$\%V_{th} = \left(\Delta V_{th} / V_{th,pre}\right) \times 100\%$$

$\%V_{th}$ should not exceed ±5%.

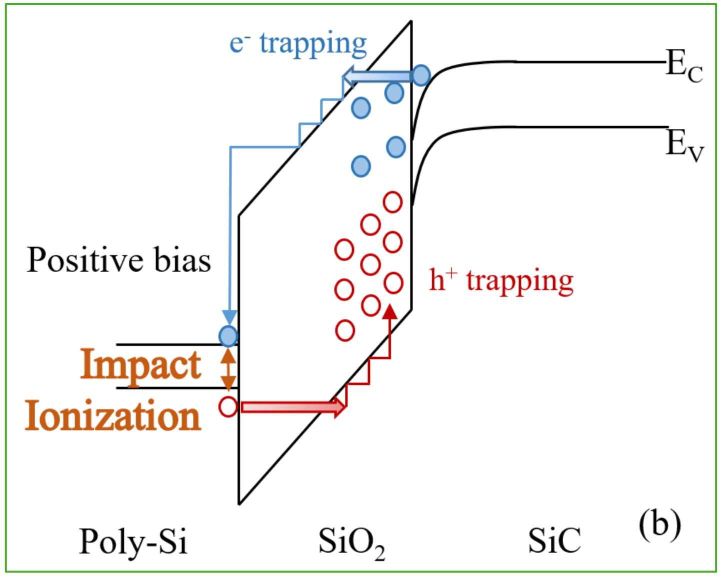
Conventional Gox Screening

Electron Trapping
Positive V_{th} shift



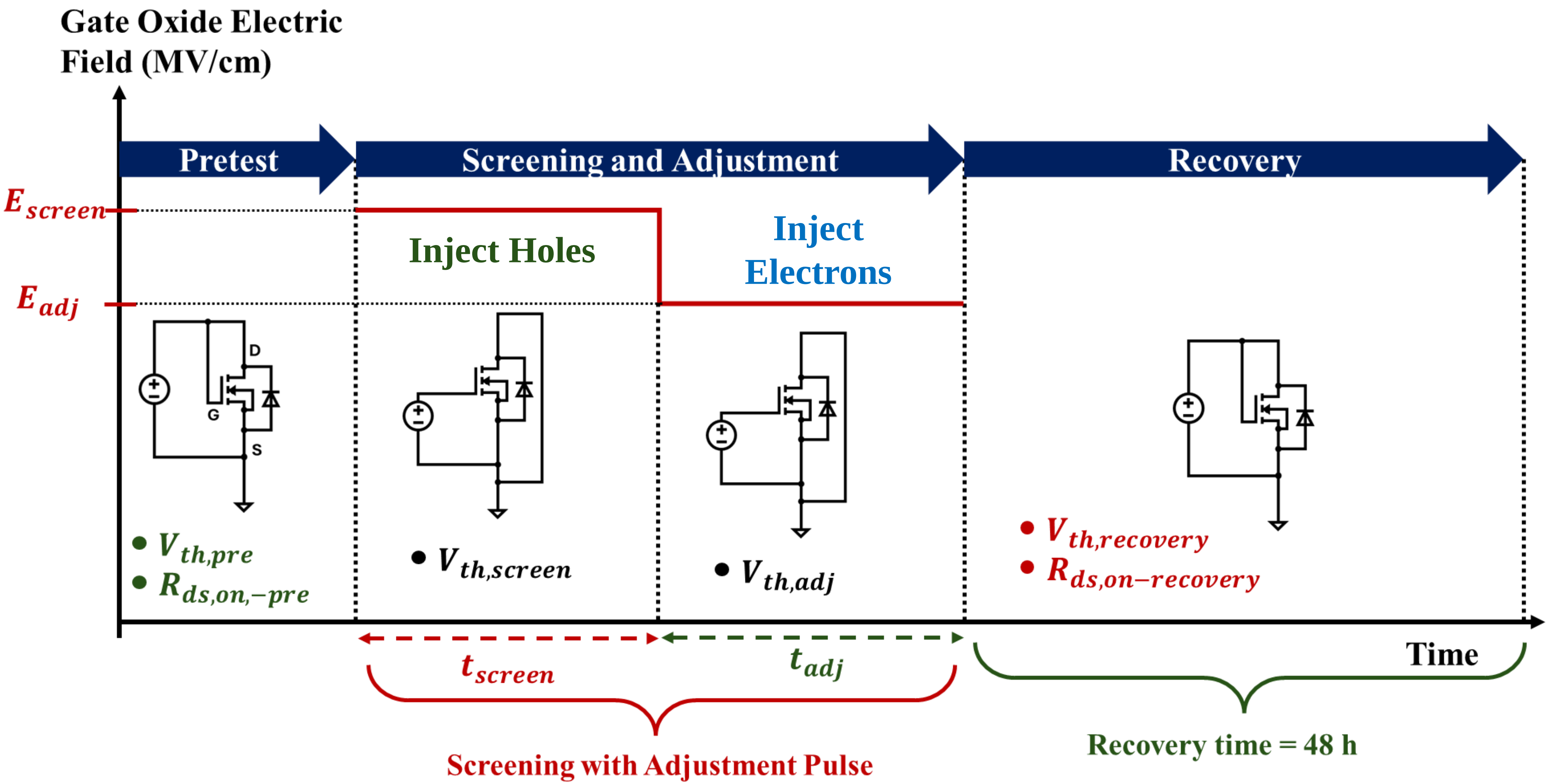


Hole Trapping
Negative V_{th} shift



$$E_{ox} = \frac{V_g}{t_{ox}}$$

Screening with Adjustment Pulse (SWAP) Technique

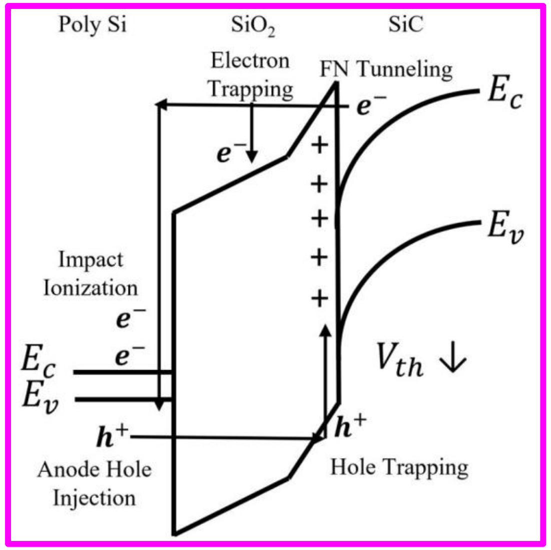


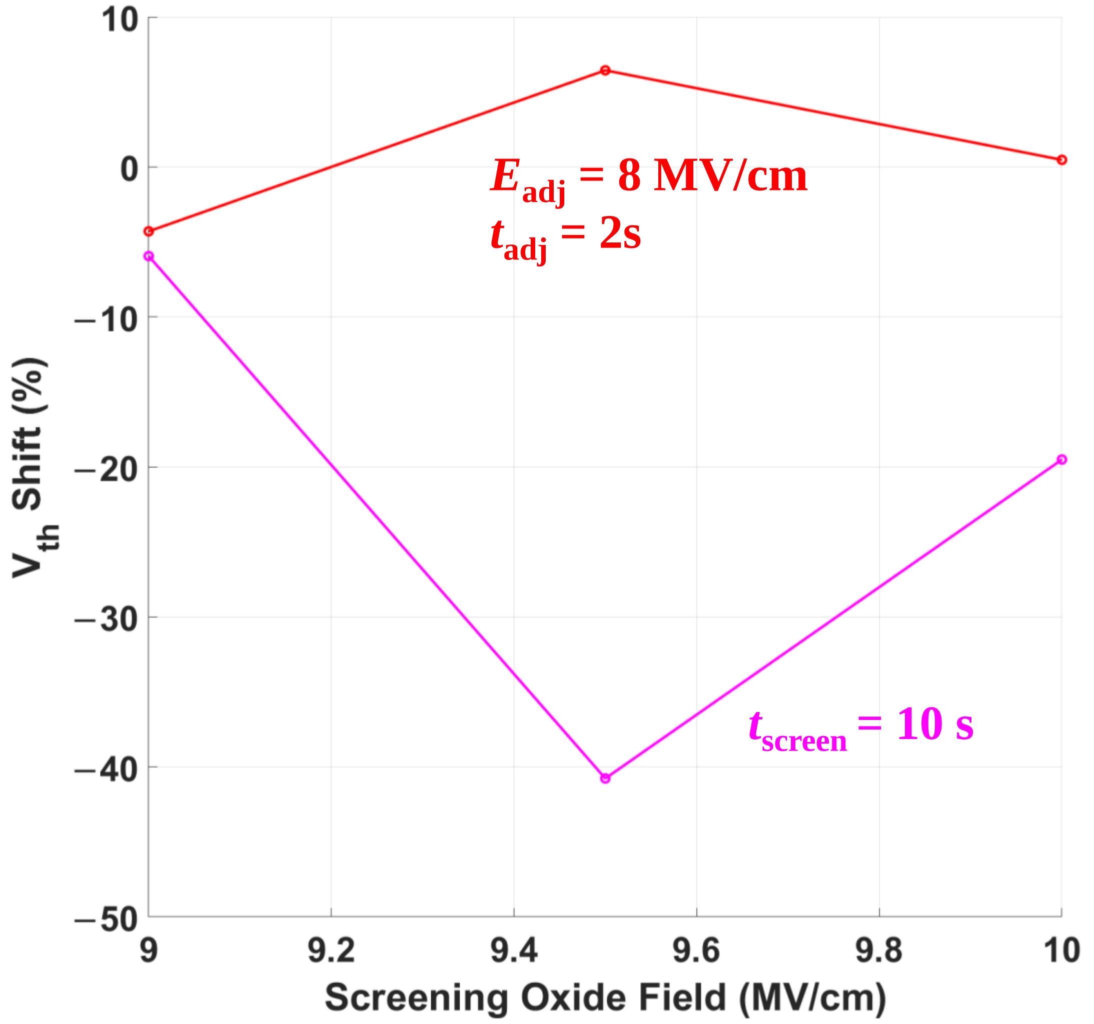
$$\Delta V_{th,SWAP} = V_{th,recovery} - V_{th,pre}$$

[2] Jin, Michael, et al. "Investigation of the Effect of Gate Oxide Screening with Adjustment Pulse on Commercial SiC Power MOSFETs." *Electronics* 14.7 (2025): 1366.

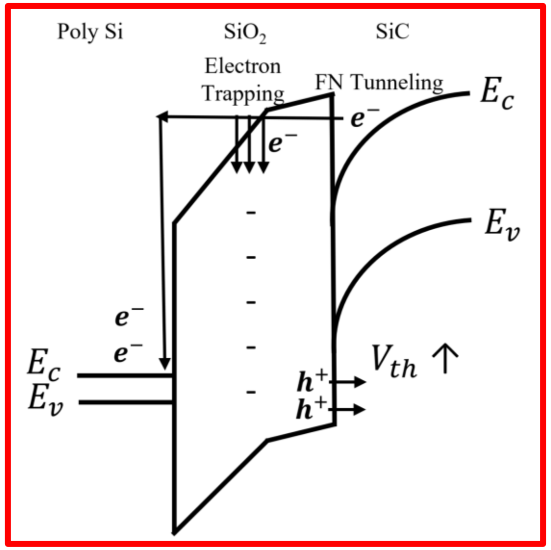
SWAP Mechanism

Hole trapping
Negative V_{th} shift

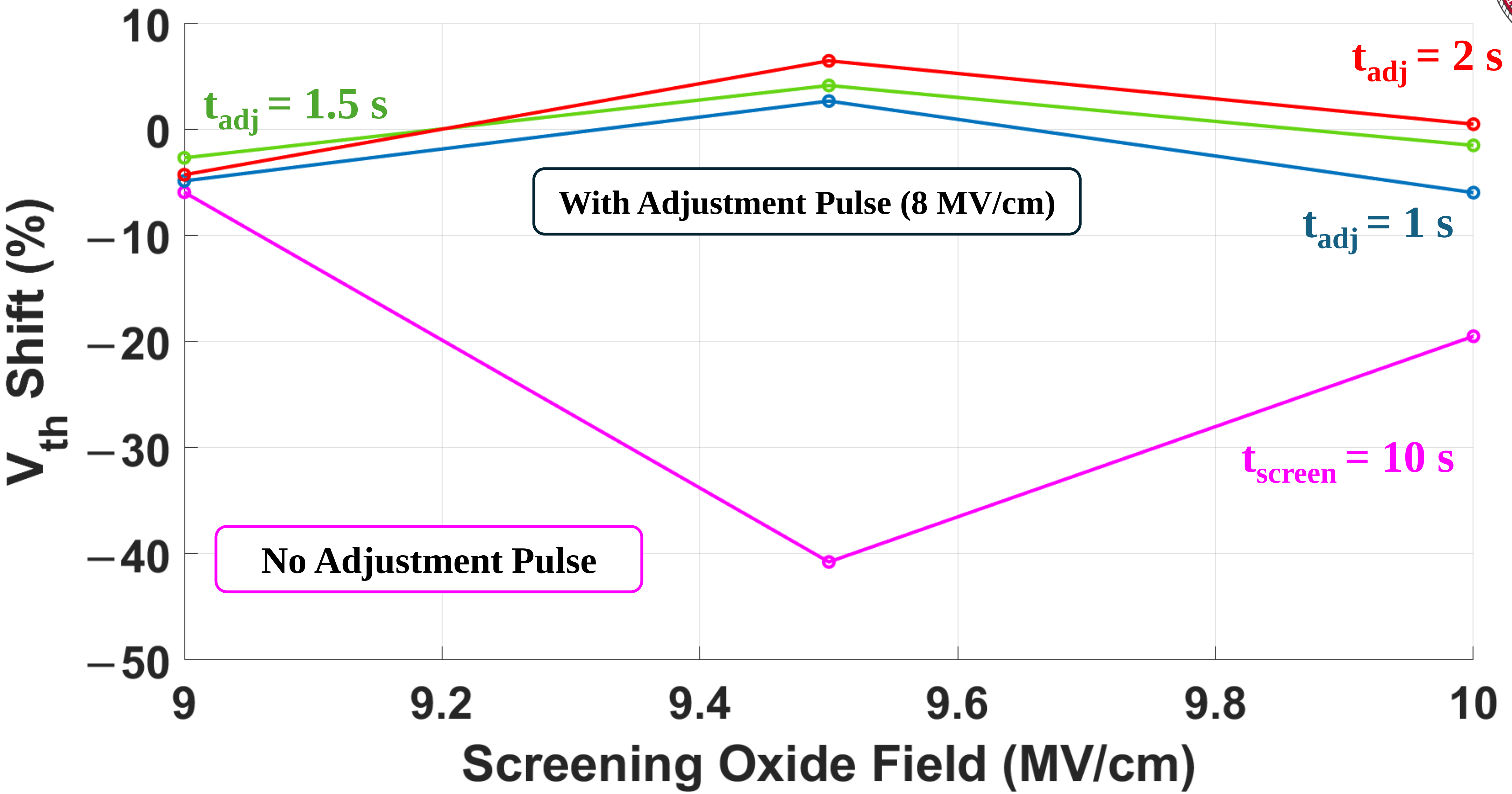




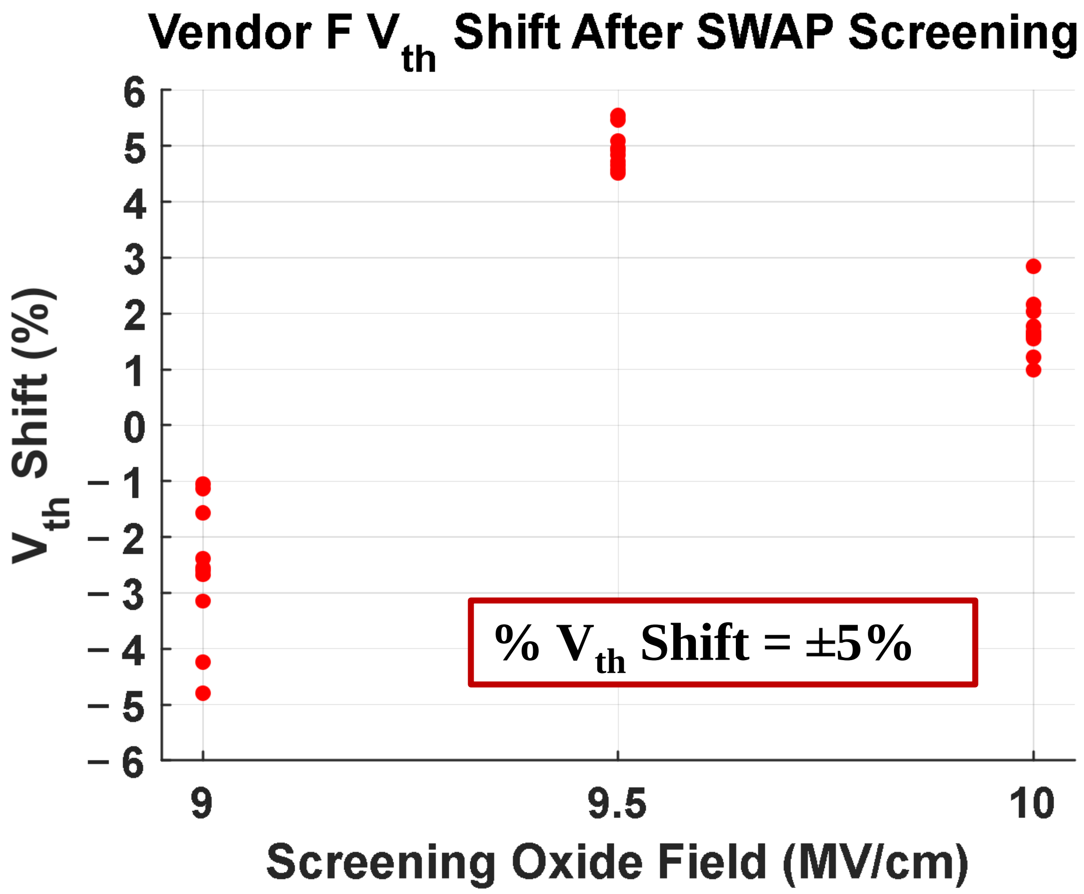
Electron trapping
Positive V_{th} shift

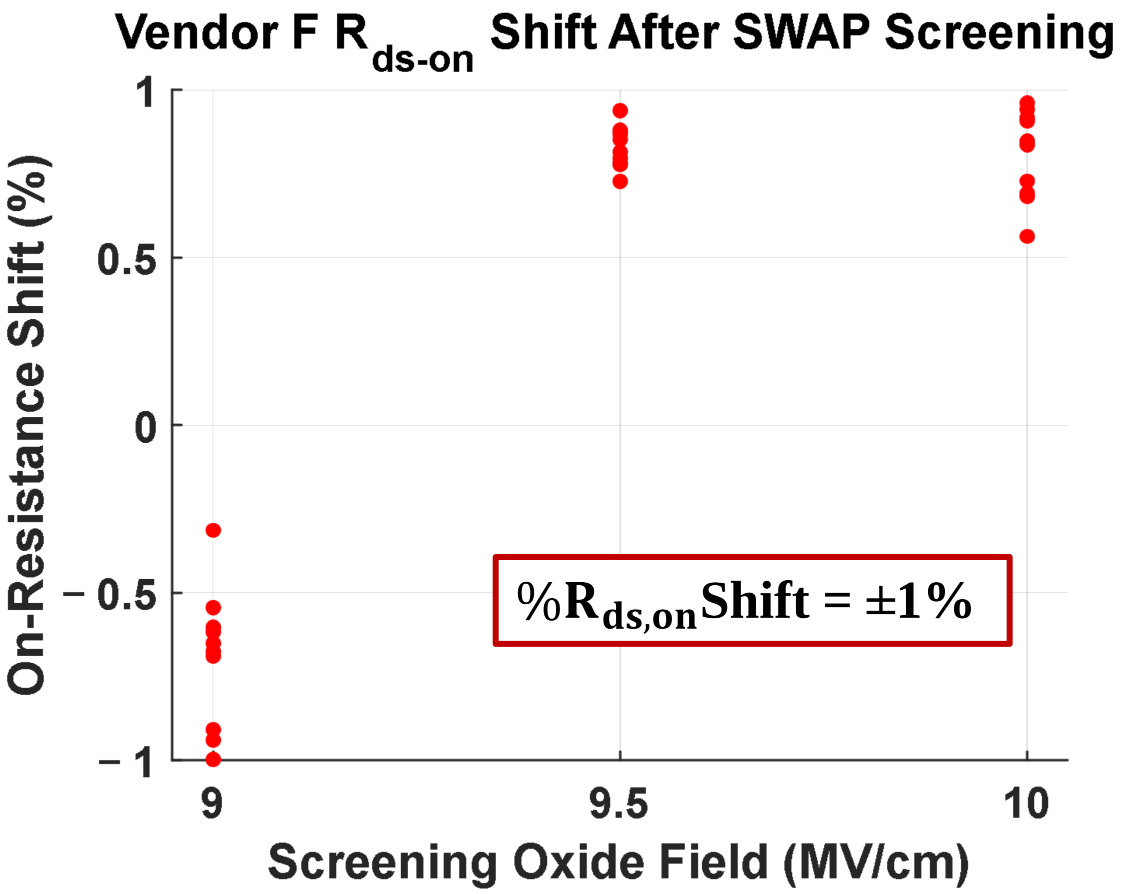


SWAP Calibration



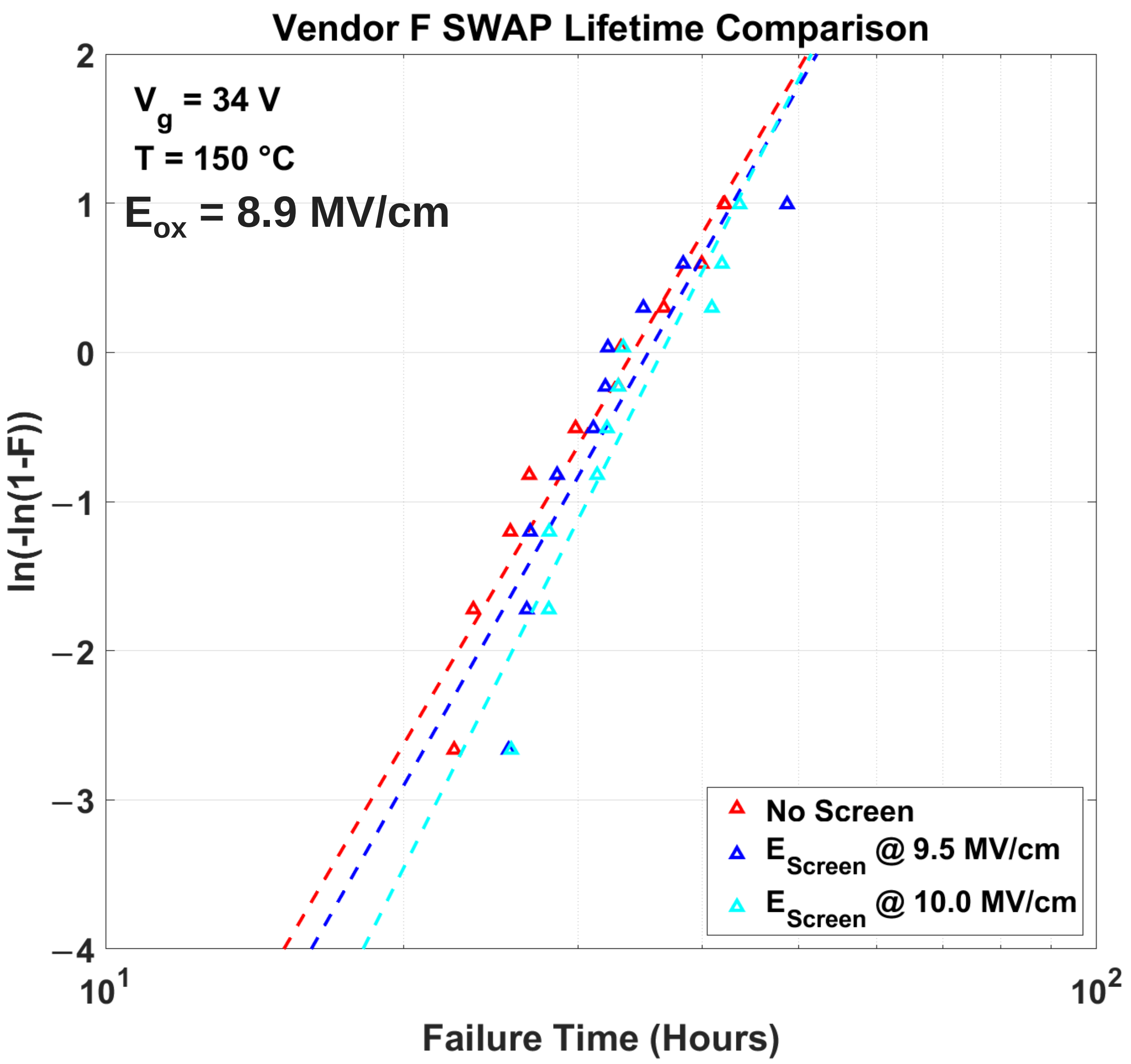
SWAP Screening Result



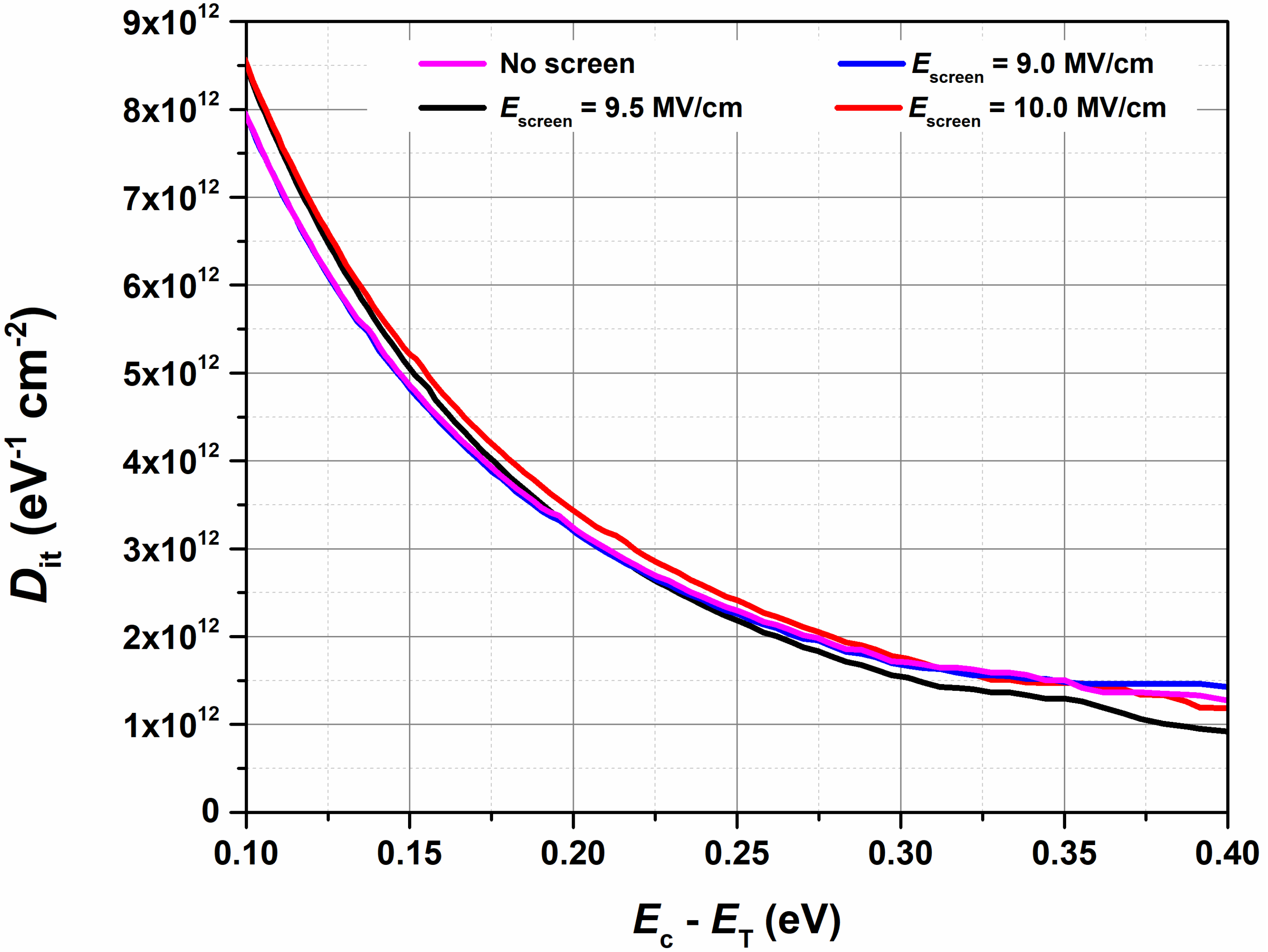


Significant increase in screening efficiency.

SWAP Screening Result: Lifetime Comparison



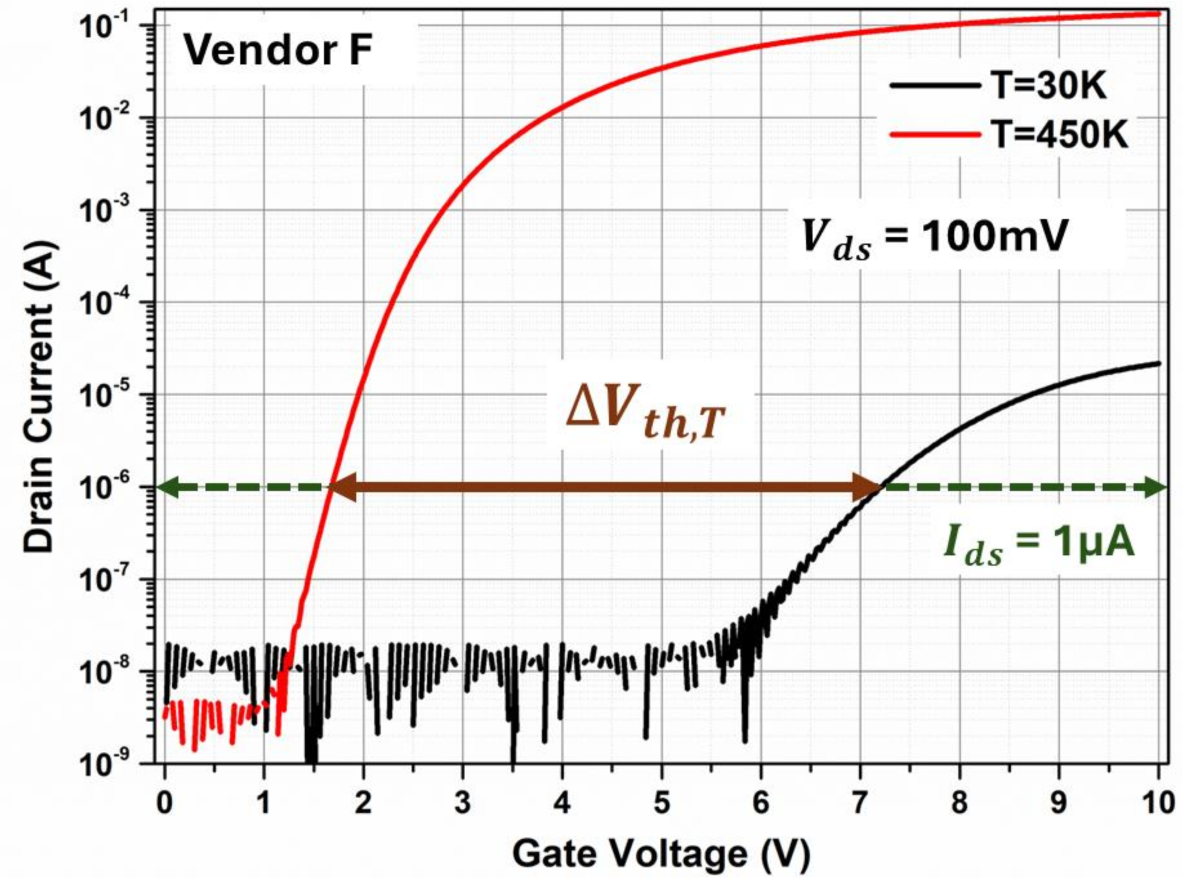
SWAP Screening Result: D_{it} Comparison: SS Method



[3] S. Yu, M. H. White and A. K. Agarwal, "Experimental Determination of Interface Trap Density and Fixed Positive Oxide Charge in Commercial 4H-SiC Power MOSFETs," in *IEEE Access*, vol. 9, pp. 149118-149124, 2021, doi: 10.1109/ACCESS.2021.3124706.

SWAP Screening Result: D_{it} Comparison: T3VS Method

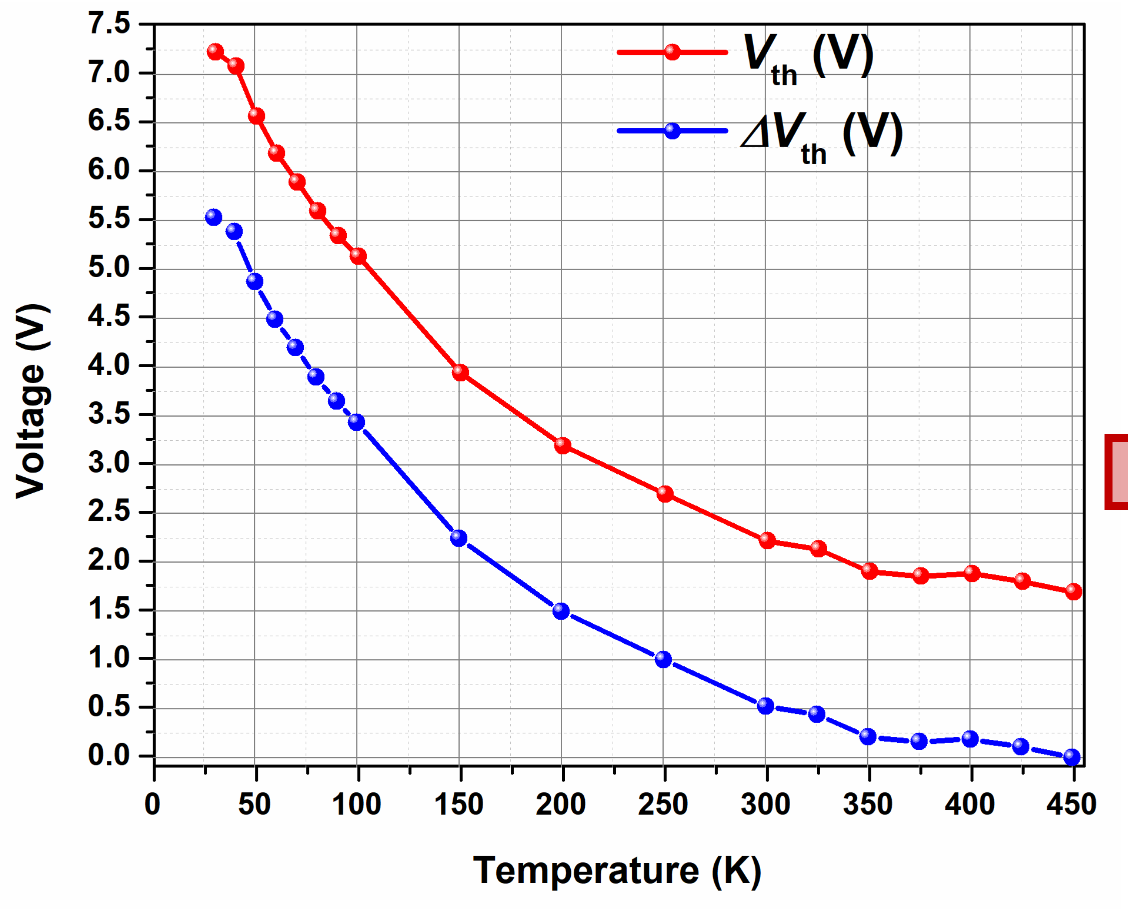
T3VS : Temperature Triggered Threshold Voltage Shift

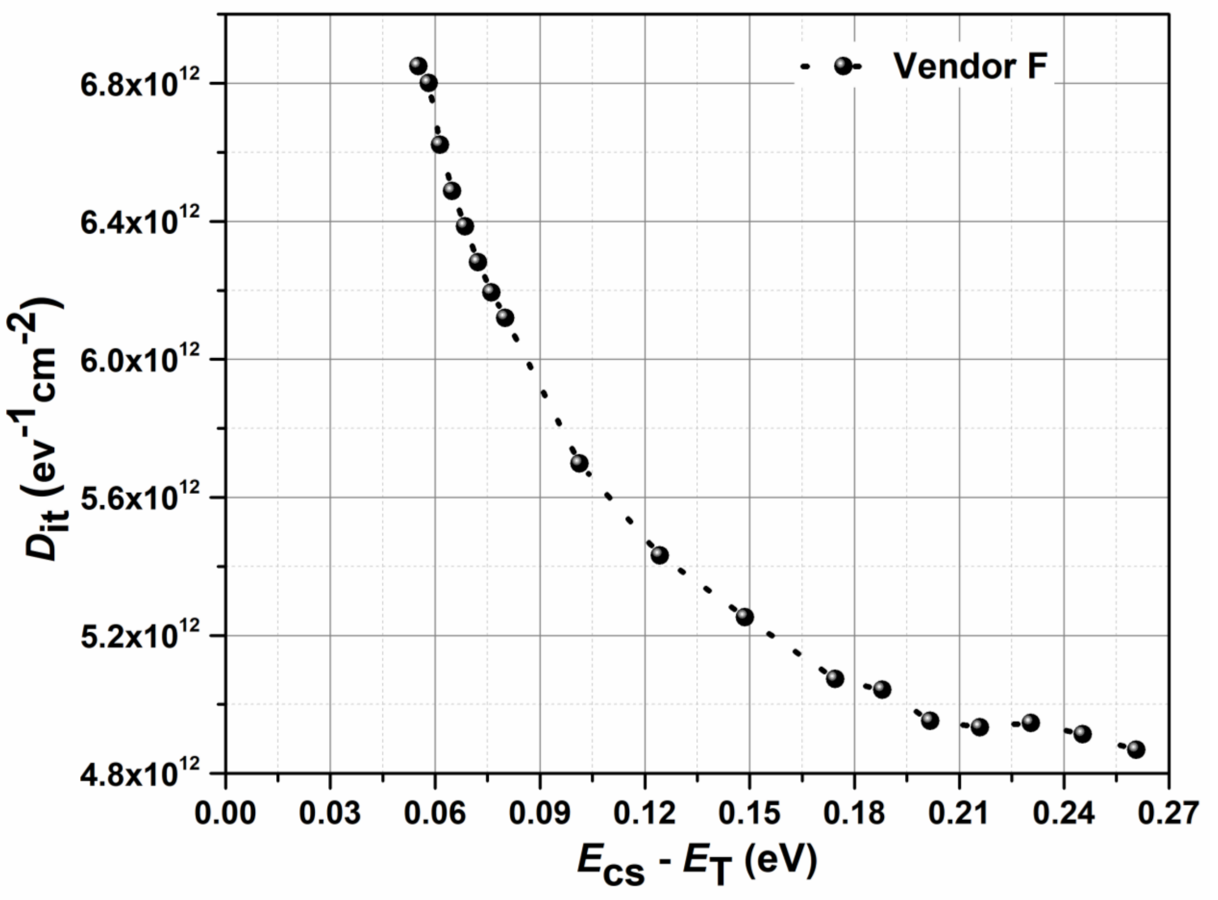


$$V_{th}(T) = f(\varphi_f(T), Q_{it}(T))$$

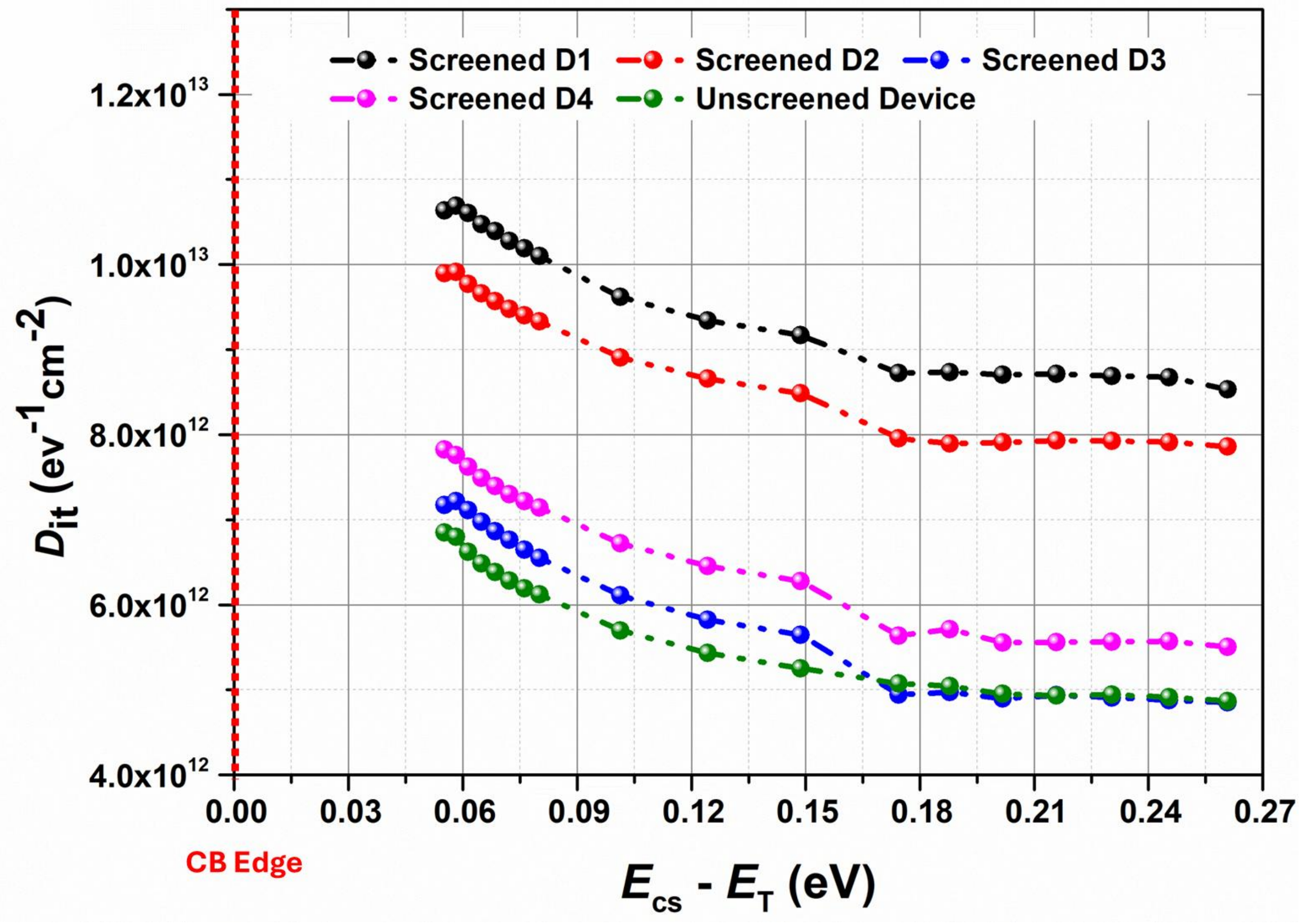
[4] Bhattacharya, Monikuntala, et al. "Analyzing the Impact of Gate Oxide Screening on Interface Trap Density in SiC Power MOSFETs Using a Novel Temperature-Triggered Method." *Micromachines* 16.4 (2025): 371.

D_{it} Extraction Methodology



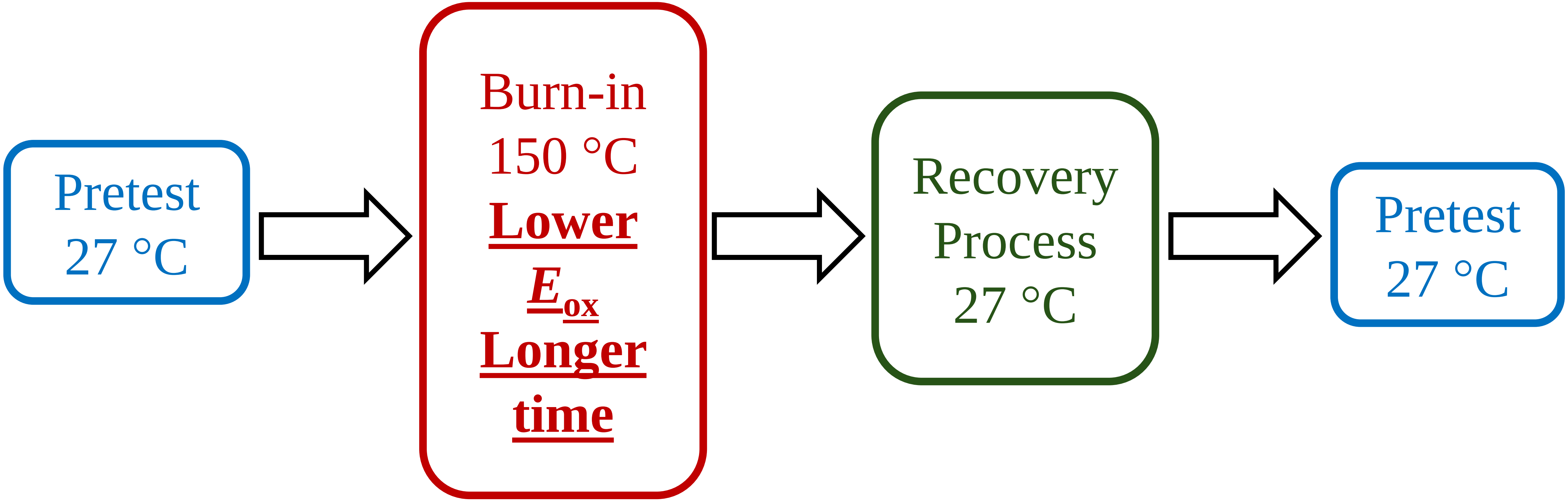


D_{it} Comparison: T3VS Method



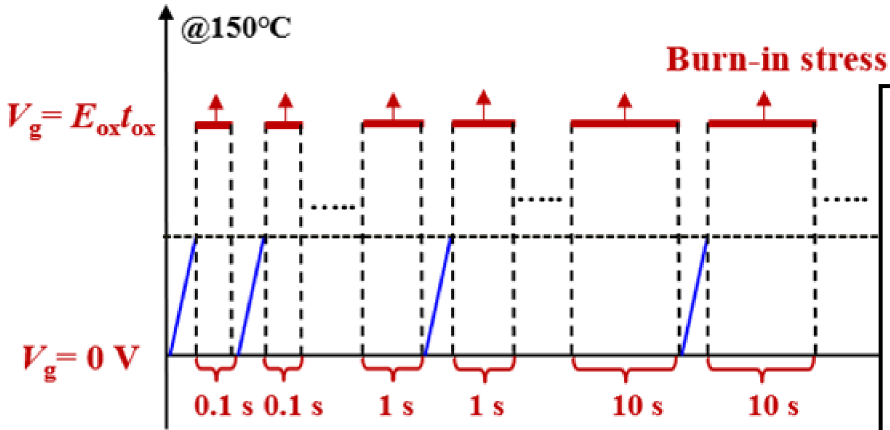
Extremely aggressive screening damage the interface of the device!

Burn-in Technique

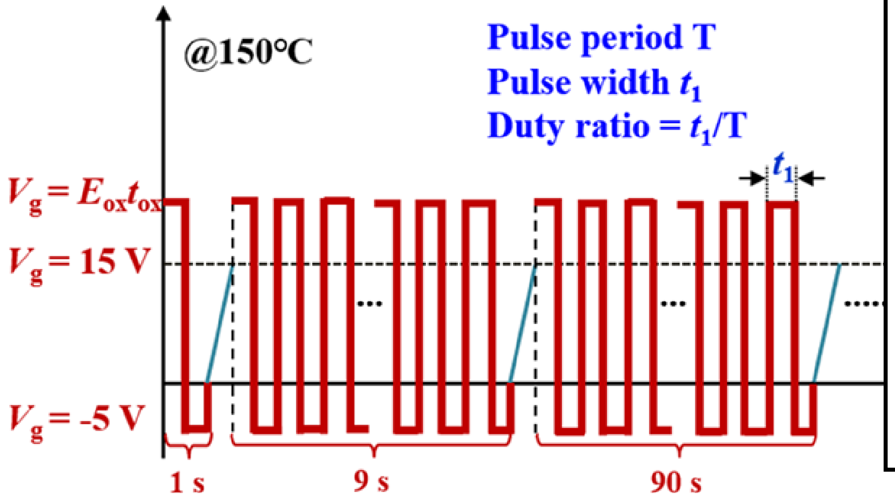


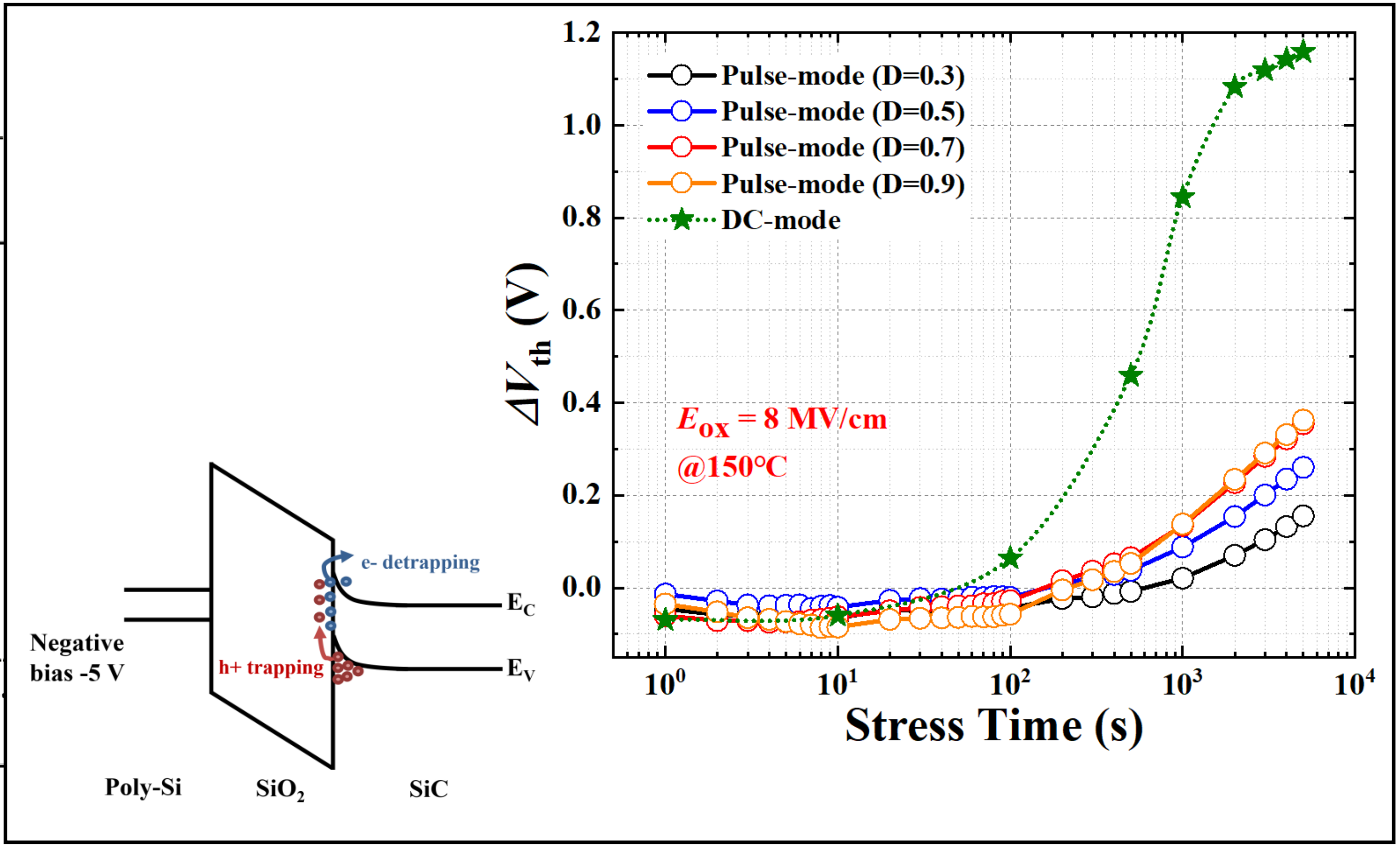
Burn-in Technique

DC Burn-in



Pulse Burn-in





[5] Shi, Limeng, et al. "Analysis and Optimization of Burn-In Techniques for Screening Commercial 1.2-kV SiC MOSFETs." *IEEE Transactions on Electron Devices* (2024).

Conclusion: GOX Screening

- In comparison to traditional gate oxide screening, screening with adjustment pulse (SWAP) is inherently more aggressive and effective.

- DC burn-in typically induces a substantial positive voltage shift in the device. The application of pulse voltage can significantly mitigate this change.

Topics

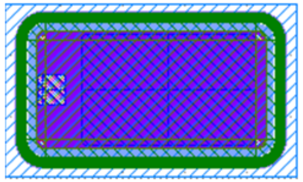
1. Analysis of Gate Oxide Screening Techniques

<u>2. Development of 3.3 kV SiC Power MOSFETs</u>

Snapshot of Device Development Protocol

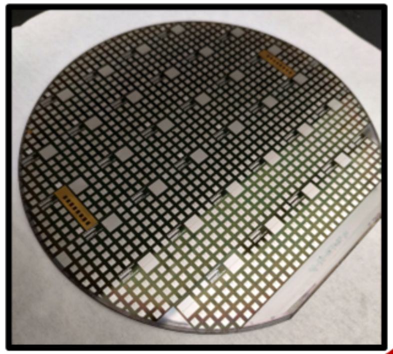
Device Design and Layout

- Simulations
  - Active Area and ET Optimization
- Mask Drawing
  - Layout Drawing
  - NoMIS Mask



Fabrication

- Commercial Foundry Clas-SiC Wafer Fab



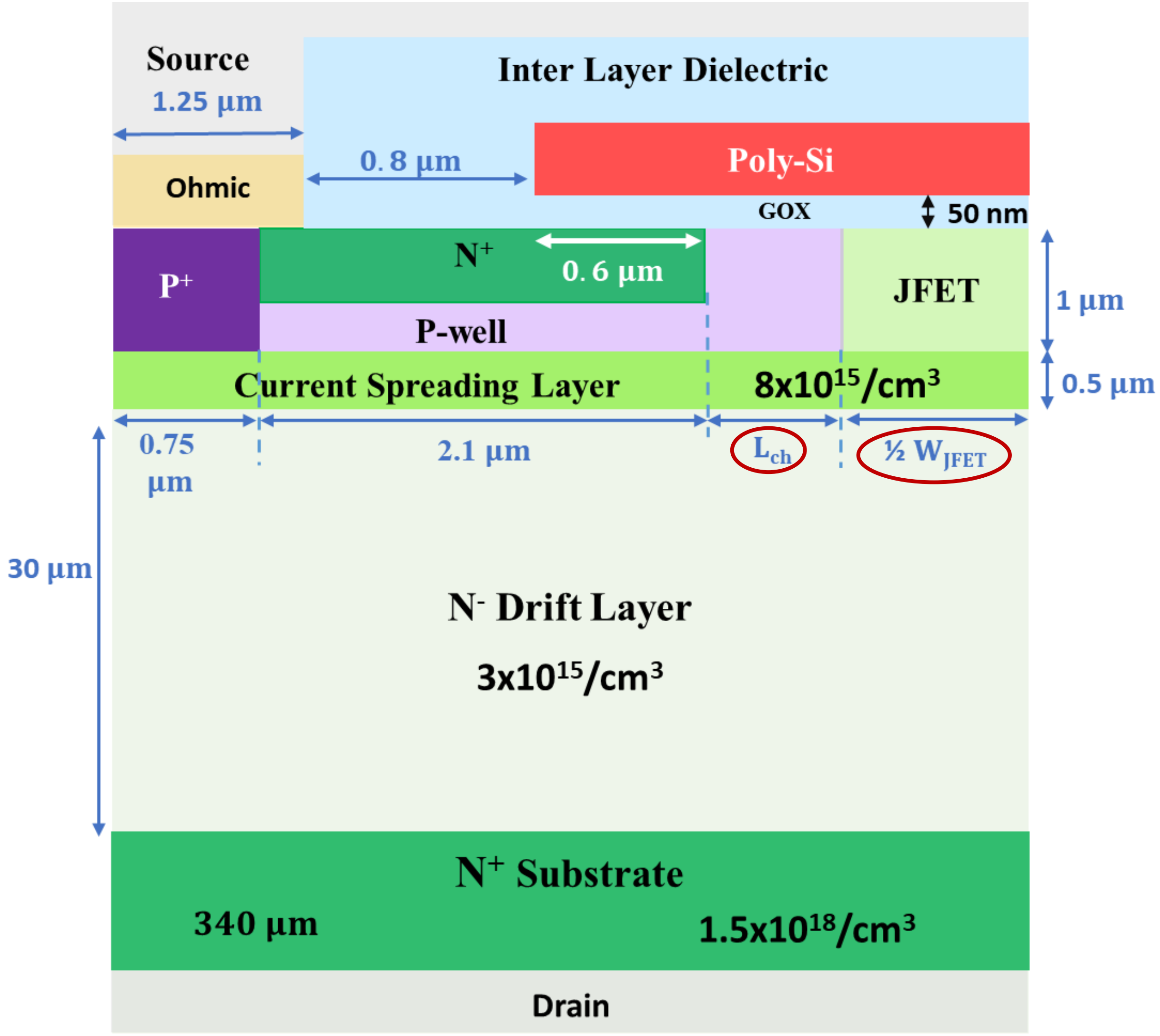
On-Wafer Testing

- Static Characterizations
  - Transfer
  - Output
  - Blocking
  - Gate-Source

Packaging and Testing

- Packaging
  - Packaged in SOT-227 package
- Testing
  - Room Temperature and High-temperature Static Measurements
  - Dynamic Measurements

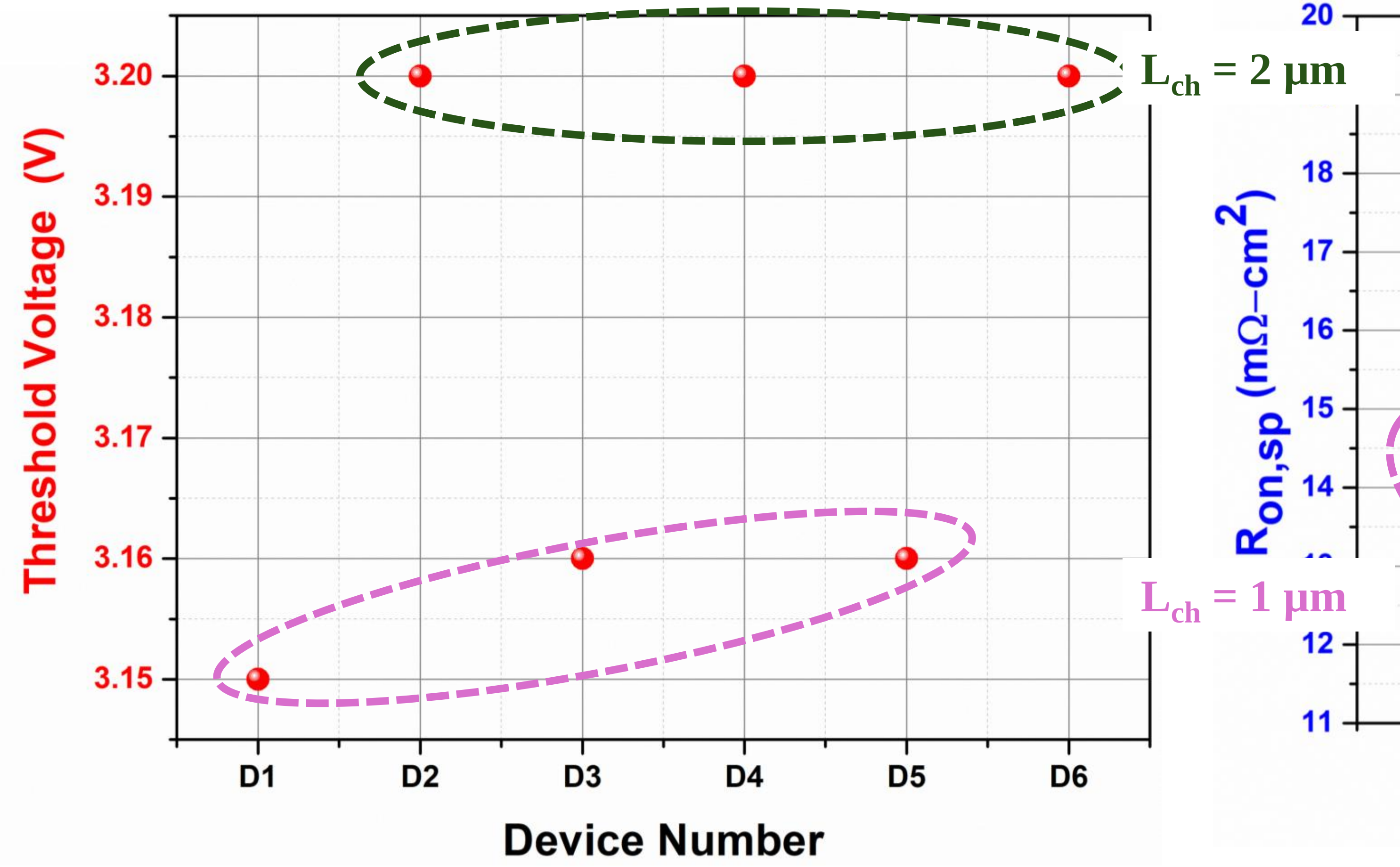
Active Area Design



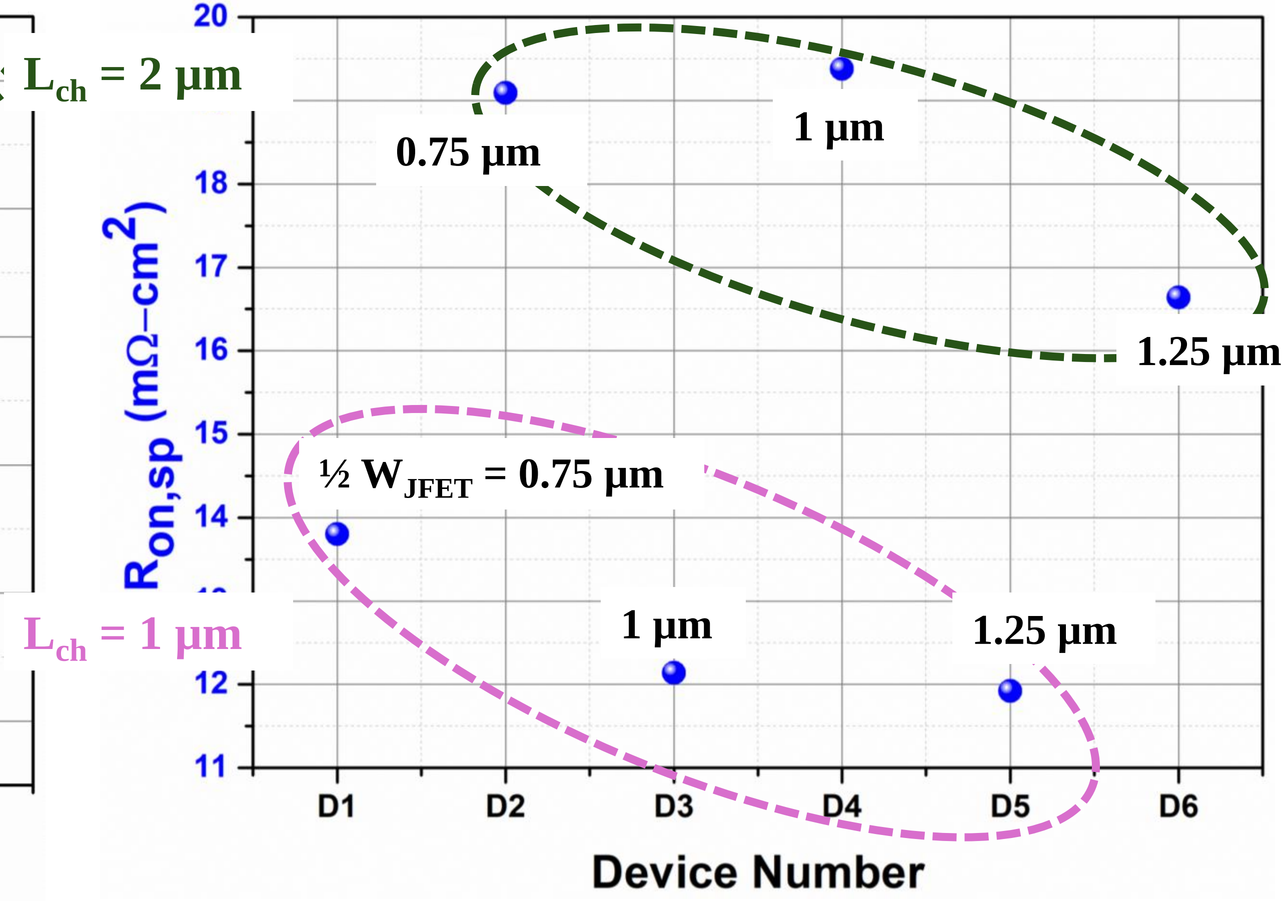
Device Number	½ W_{JFET} (μm)	L_{ch} (μm)	½ Cell Pitch (μm)
D1	0.75	1	4.4
D2	0.75	2	5.4
D3	1	1	4.65
D4	1	2	5.65
D5	1.25	1	4.9
D6	1.25	2	5.9

Simulation Result

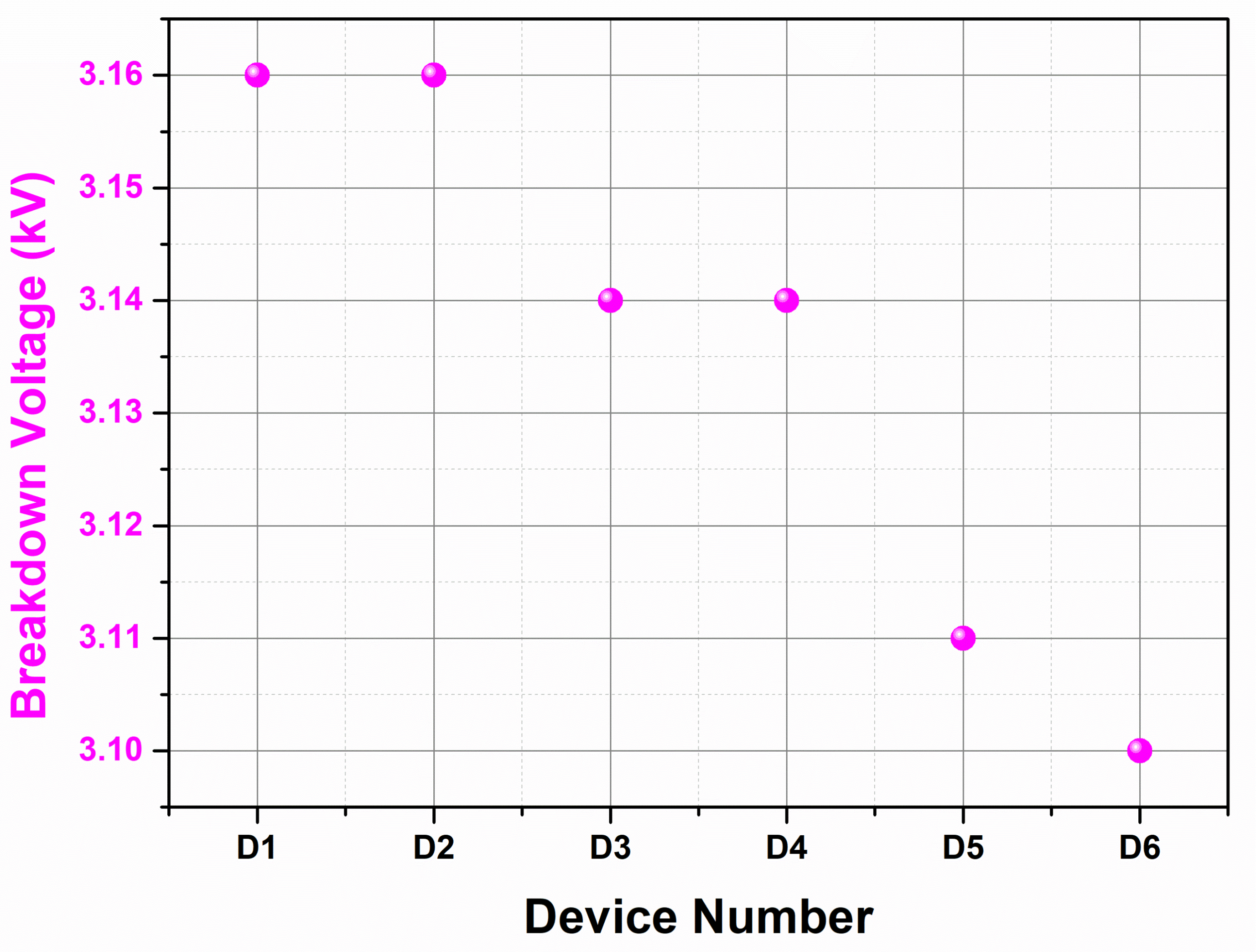
Threshold voltage: Linear Extrapolation
V_{ds} = 100 mV



On resistance : V_{gs} = 20 V and V_{ds} = 2 V
$R_{on,sp}$ = R_{on} x P/2 µm x 1 µm

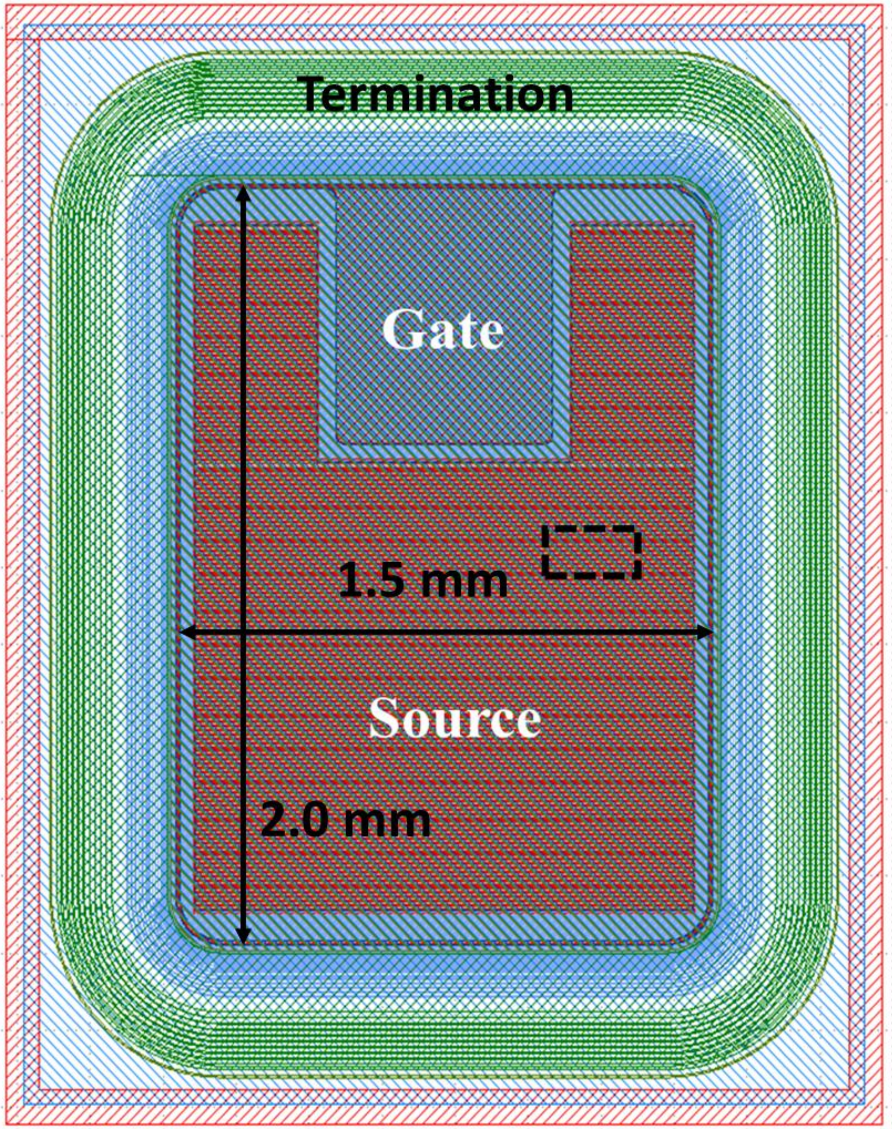


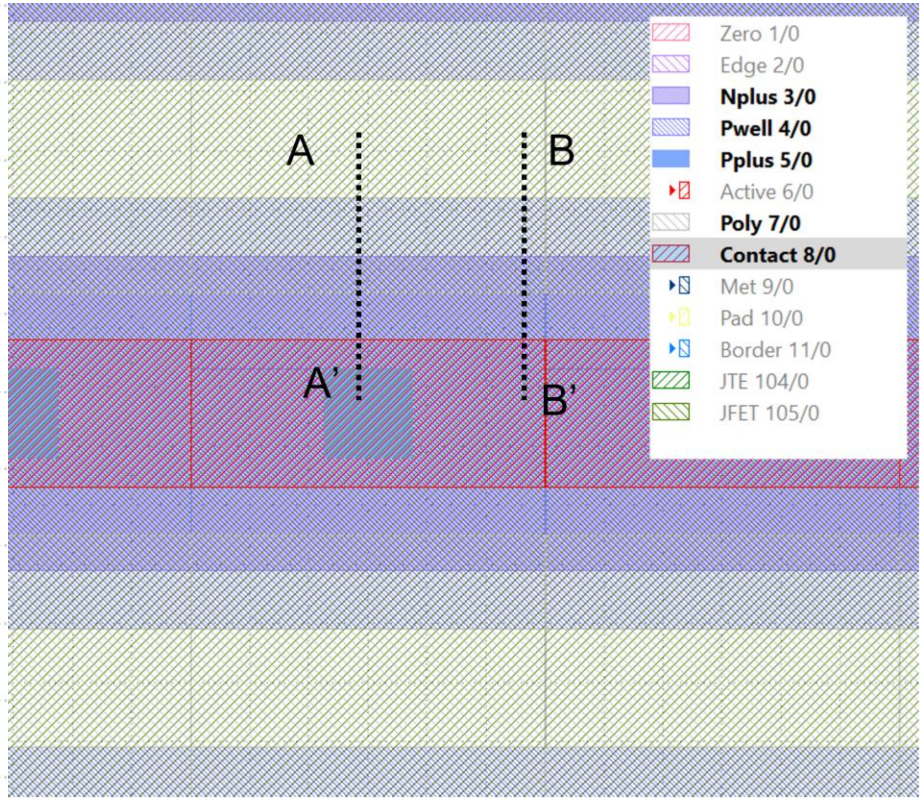
Simulation Result

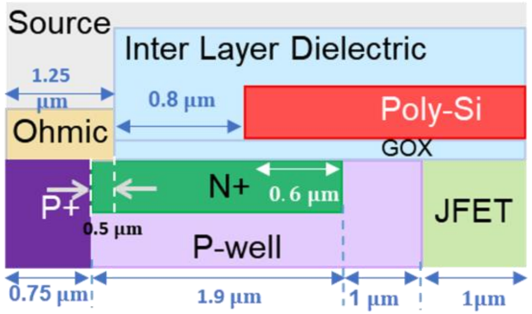


- Drift layer design only supports a breakdown voltage of ~3.1 kV.
- Introduce termination structure to fully utilize the high voltage blocking capability.

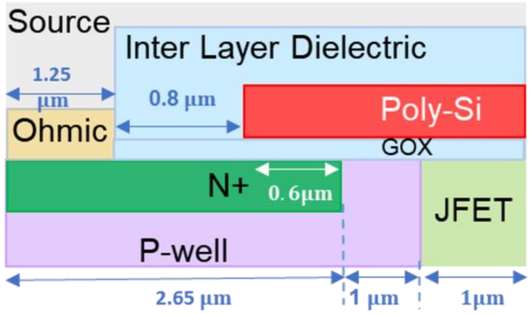
A Sample Layout







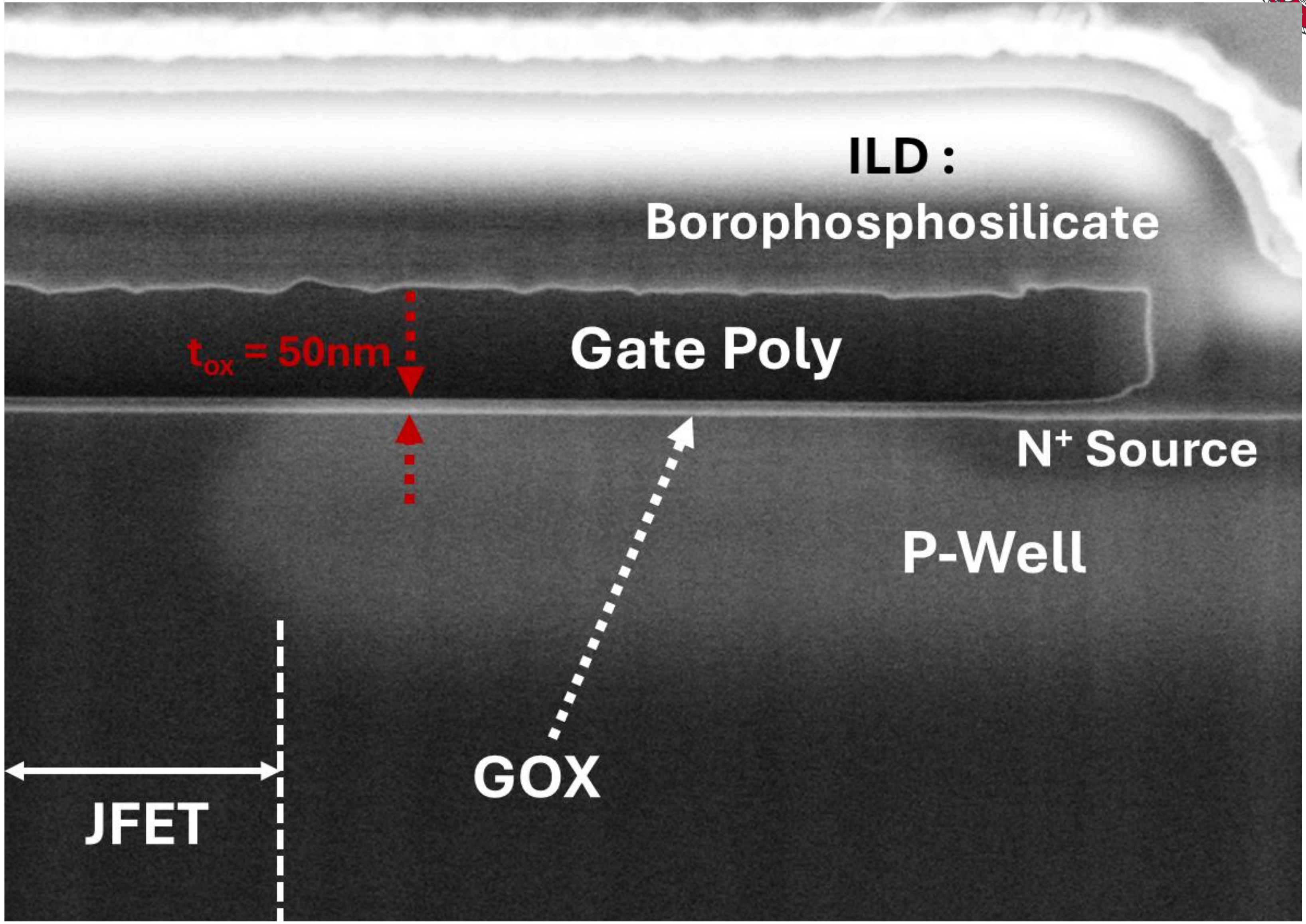
Cutline Along A-A'



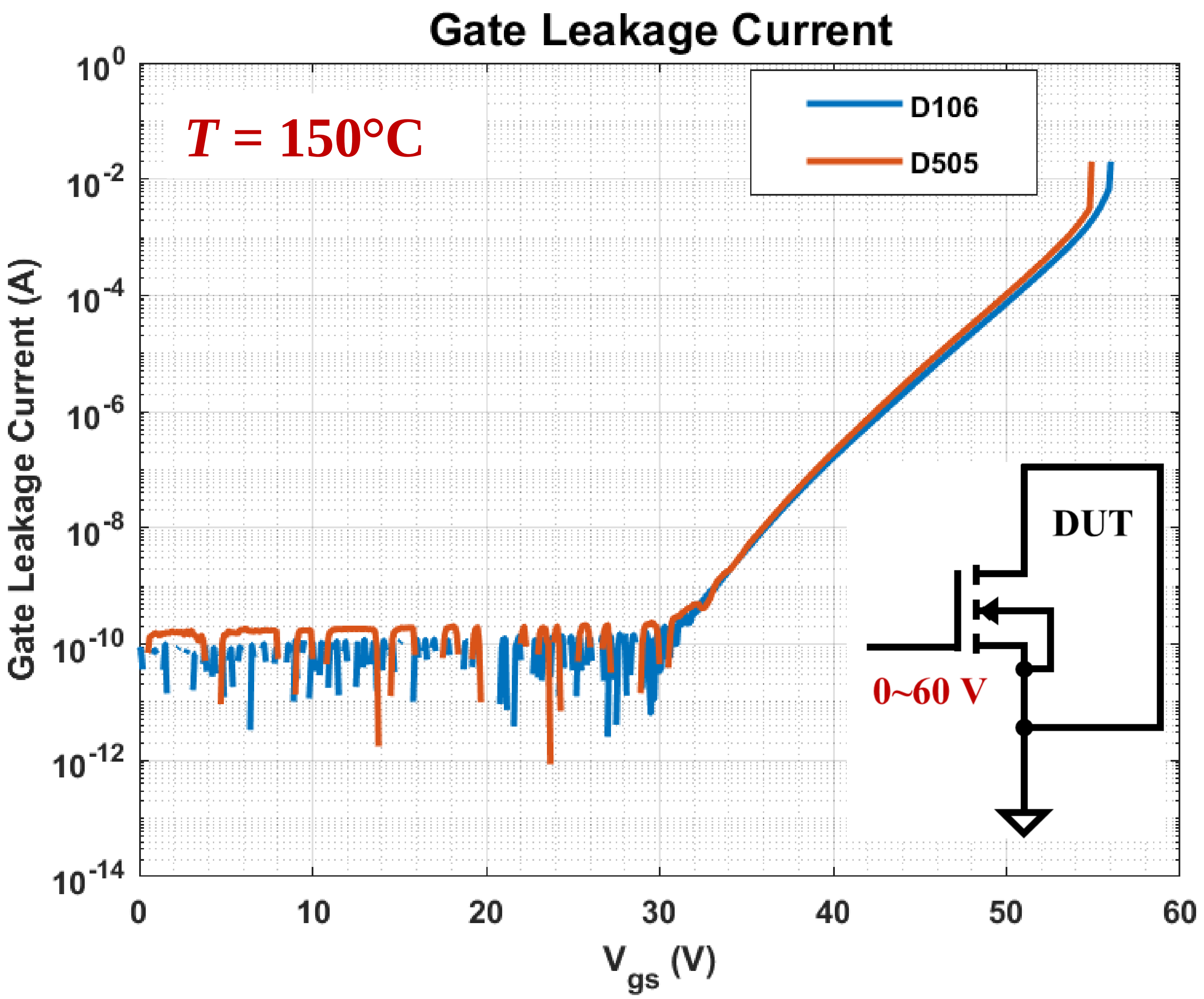
Cutline Along B-B'

- Horizontal stripped cell
- Orthogonal P^+ contact to reduce R_{on} by reducing cell pitch

Fabricated Device Structure



Extraction of Gate Oxide Thickness



$$t_{ox} = \frac{V_{br}}{E_{ox}}$$

E_{ox} = 11 MV/cm

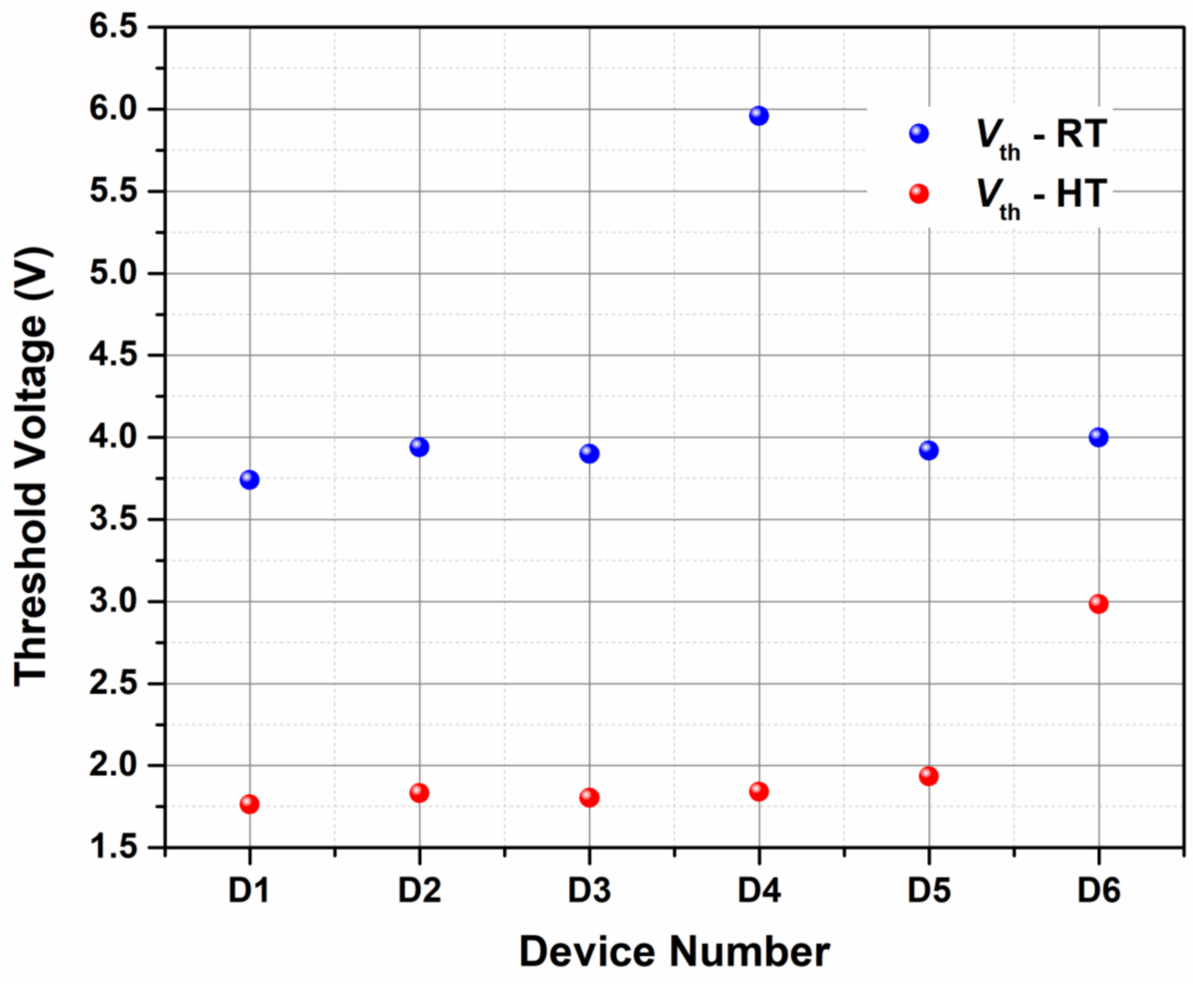
Device	V_{br} (V)	t_{ox} (nm)
D106	55.9	50.82
D505	54.8	49.82

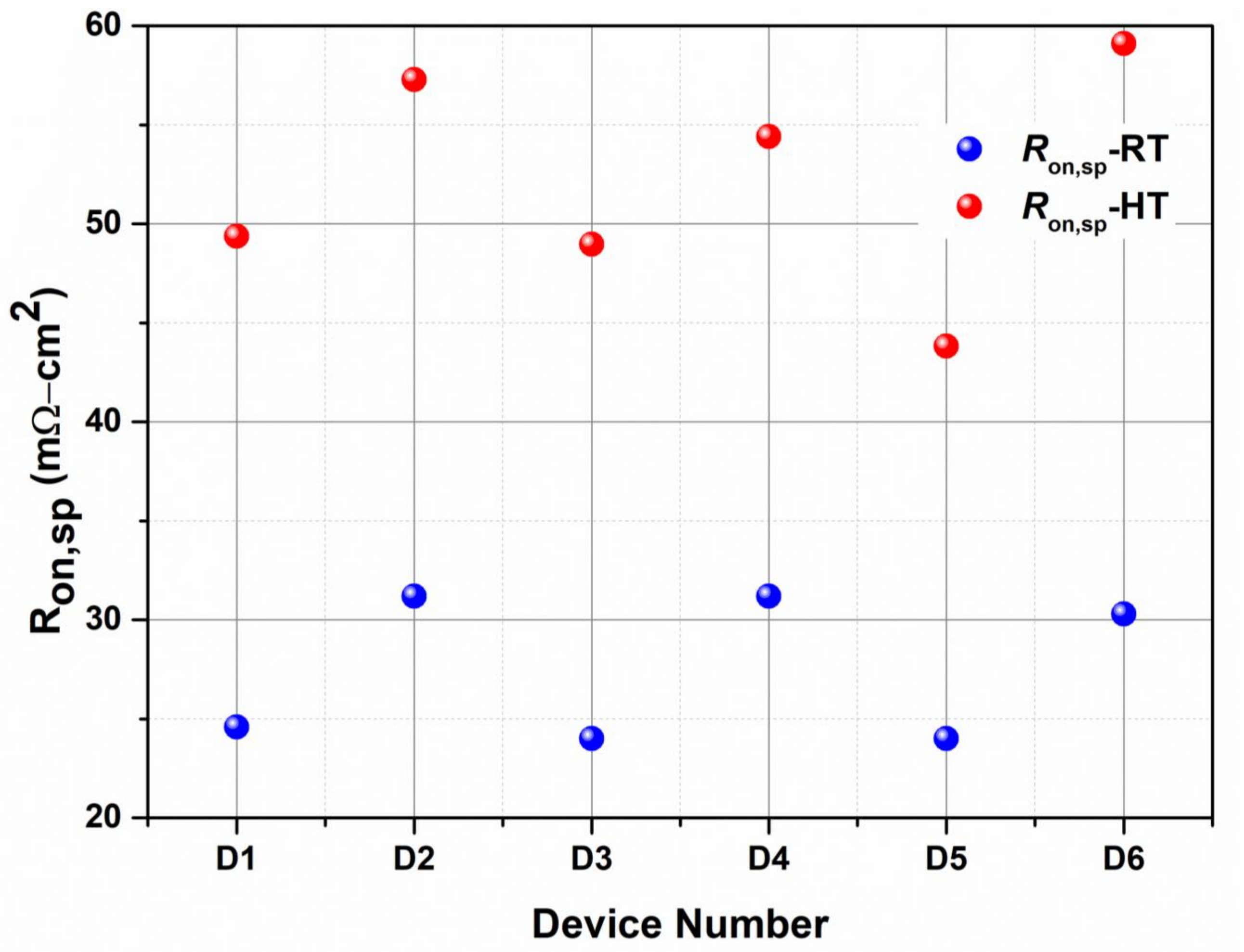
[6] Shi, Limeng, et al. "Gate Oxide Reliability in Silicon Carbide Planar and Trench Metal-Oxide-Semiconductor Field-Effect Transistors Under Positive and Negative Electric Field Stress." *Electronics* 13.22 (2024): 4516.

RT and HT (150°C) Static Measurements

Linear Extrapolation Method
V_{ds} = 100 mV

V_{gs} = 20 V; V_{ds} = 2 V
$R_{on,sp}$ = R_{on} x 1500 μm x 2000 μm





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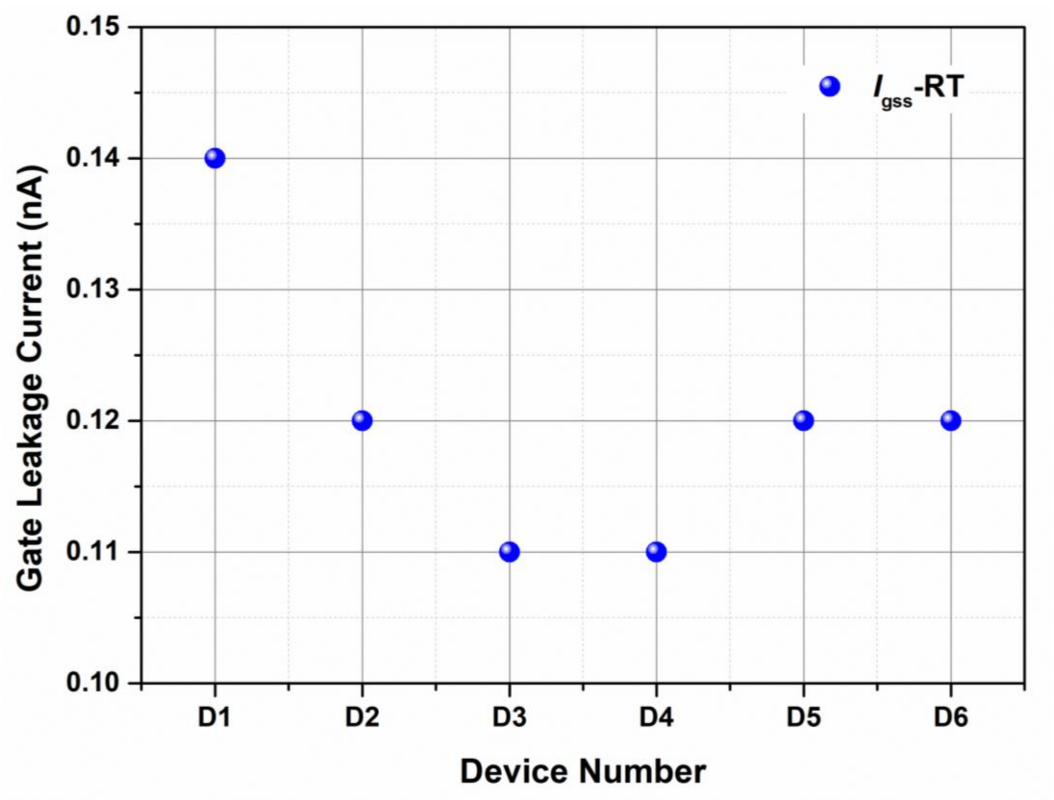
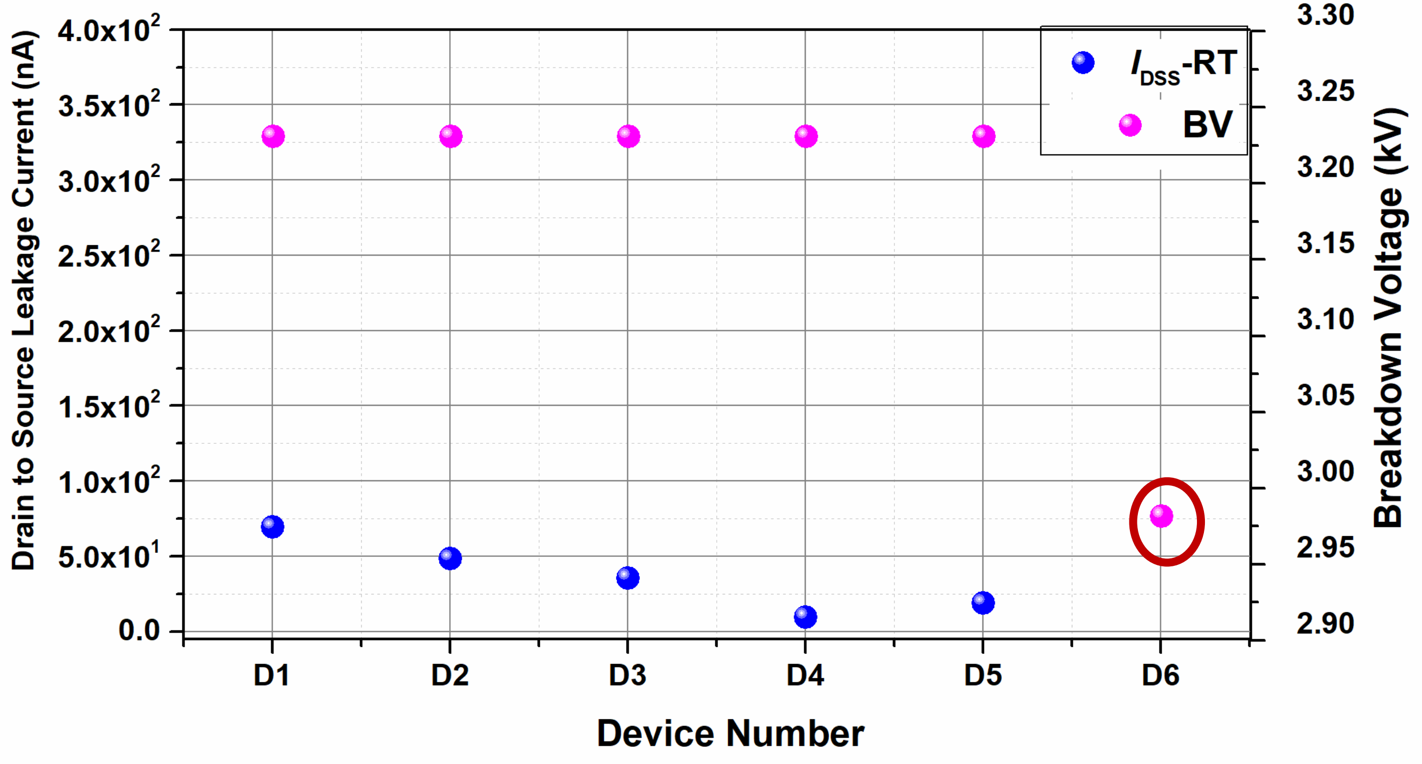
V_{gs} = 30 V; E_{OX} = 6 MV/cm



V_{ds} = 3.0 kV



Conclusion : Development of 3.3 kV MOSFET

- Successfully simulated and designed 3.3 kV SiC MOSFET.

- Experimental results align with the simulated results.

- Deliver comprehensive training on device design, highlighting future aspects of optimization for enhanced performance and reliability.

Thank You!

Any Questions?

Self-Introduction

Monikuntala Bhattacharya

- PhD candidate in the Department of Electrical and Computer Engineering at the Ohio State University under supervision of Prof Anant K. Agarwal since Jan,2022. Completed Summer Internship at Clas-SiC's Foundry.
- B.Tech. (B.S.) degree in Electrical Engineering from Maulana Abul Kalam Azad University of Technology, India, 2017.
- M. Tech. (M.S.) degree in Nanoscience and Technology from Jadavpur University, India, 2019.
- Research Topic: Advancing SiC MOSFET Reliability: Non-destructive Short Circuit Screening, Interface State Analysis and Device Design Insights.
- SiC MOSFET device design, short circuit reliability, cryogenic characterization and interface analysis, gate oxide screening, BTI and TDDB Technique.
- Notable Publications

1. Bhattacharya, Monikuntala, et al. "**Analyzing the Impact of Gate Oxide Screening on Interface Trap Density in SiC Power MOSFETs Using a Novel Temperature-Triggered Method**." *Micromachines* 16.4 (2025): 371.
2. Bhattacharya, Monikuntala, et al. "**A Non-destructive Short Circuit Withstand Time Screening Methodology for Commercially Available SiC Power MOSFET**." *2024 IEEE 11th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*. IEEE, 2024.

- Presentations

1. "Investigation of Interface Traps Distribution using a Temperature Dependent Threshold Voltage Shift Method in Commercial 4H-SiC Power MOSFETs", *ICSCRM*, 2024, NC, USA.
2. "3.3-kV SiC Device Development", *CHPPE Annual Review*, 2024, OH, USA.
3. "Reliability Investigation and Screening Technology for the Gate Oxide in Commercial SiC power MOSFETs", *The 8th US-Japan Digital Innovation Hub and Advanced Technology Workshop*, 2024, OH, USA.