Long-Wavelength 1550nm VCSELs for Optical Communication and FMCW LiDAR

Coherent/II-VI Foundation Mini-Conference

Kevin P. Pikul, Ph.D.
Emily Becher
Jason Flanagan
PI: John Dallesasse

Department of Electrical and Computer Engineering, Grainger College of Engineering
University of Illinois at Urbana-Champaign
Nick Holonyak, Jr. Micro and Nanotechnology Laboratory

Introductions: Group Members

Kevin Pikul, Ph.D.

B.S. (2018), M.S. (2021), Ph.D. (2025)
VCSEL Design, Fabrication, and Characterization (Anti-Phase Coatings and IID)

Leah Espenhahn

B.S. (2020), Ph.D. (Current)
VCSEL Design, Fabrication, and Characterization (Anti-Phase Coatings)

Emily Becher

B.S. (2024), M.S. (Current)
Long-Wave VCSEL Fabrication

Jason Flanagan

B.S. (2024), M.S. (Current)
Long-Wave VCSEL Simulation

Robert Kaufman, Ph.D.

B.S. (2017), M.S. (2021), Ph.D. (2025)
TI-QCL Design, Fabrication, and Characterization

Anik Mazumder

B.S. (2023), M.S. (2025), Ph.D. (Current)
TI-QCL Design, Fabrication, and Characterization

Research Group Capabilities

Heterogeneous Integration Methods

- Methods for epitaxial transfer of III-V materials onto silicon have been developed in the Dallesasse Research Group
- Transfer method results in top epitaxial layer facing “up” after transfer, facilitating device fabrication after transfer
- Precise positioning of III-V material in a wafer-scale process
- Thickness of transferred material can be precisely controlled

Photonic Devices

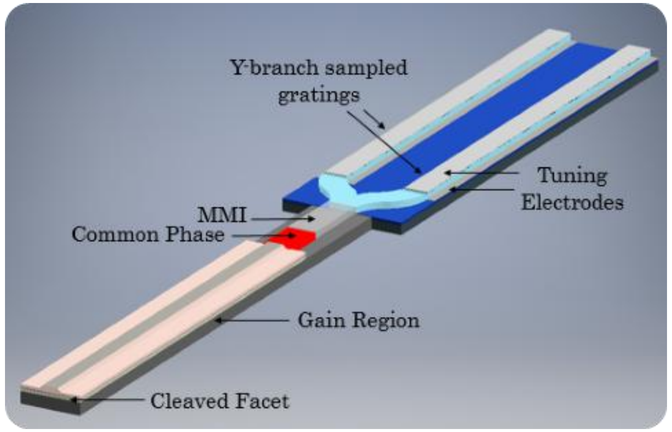
- Design and fabrication of mid-IR emitters for sensing systems (quantum cascade)
- VCSEL mode control for LIDAR/3D Imaging/Data Center

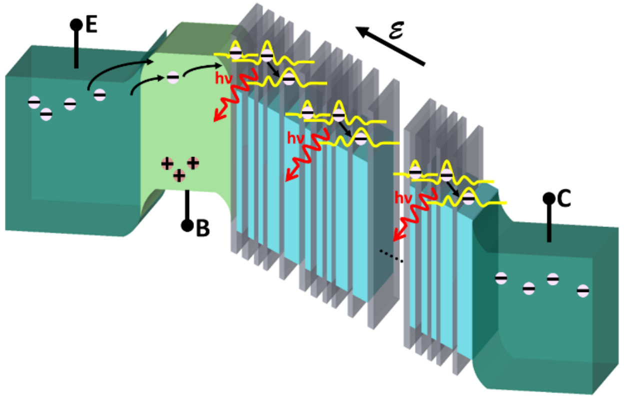
Nitride Photonics

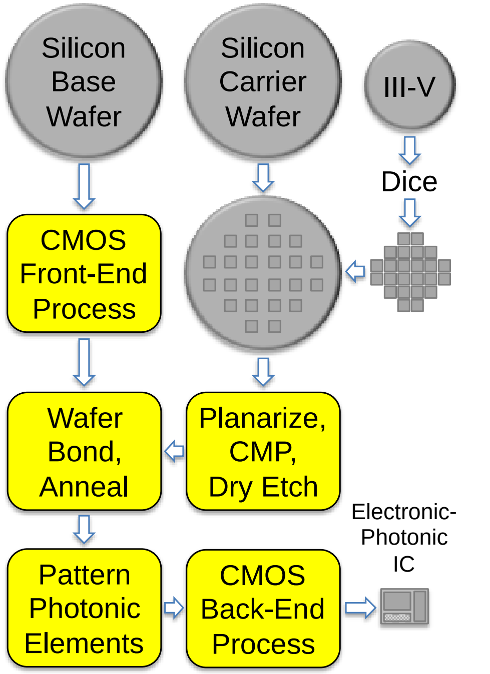
- Preliminary work on photonic integration using arsenide/phosphide gain material heterogeneously integrated with III-N material for photon control
- Device designs have been examined for MZMs, tuning elements for tunable lasers, electrically-controlled polarization rotators
- Low static power dissipation – field-controlled devices
- Mn in III-N materials – photon control of spin state, possible quantum information application

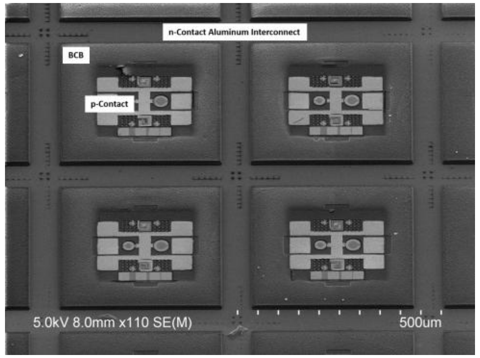
Modeling Capabilities

- Band structure calculations for III-N materials, photonic device modeling (waveguides, coupling structures, DBRs, Schrodinger-Poisson solvers), strained quantum dots



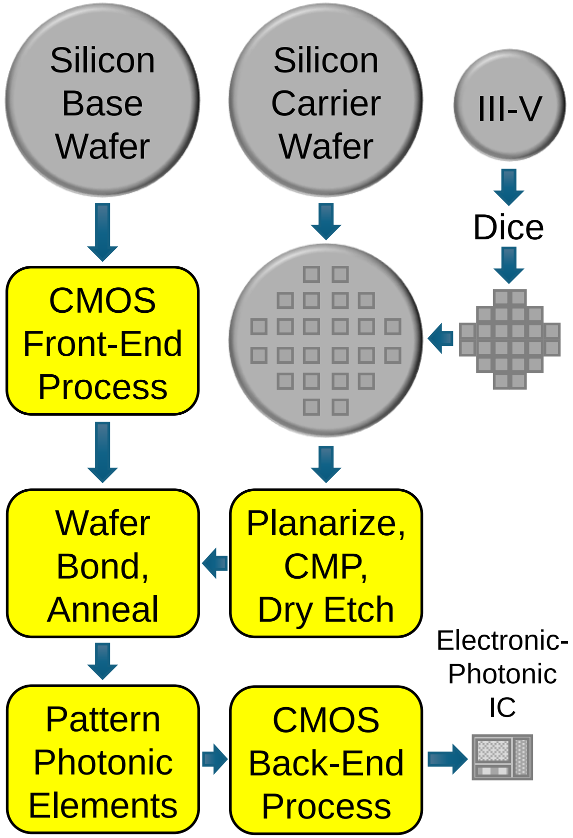




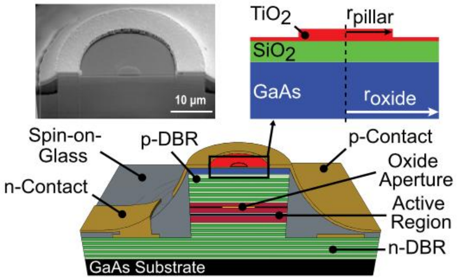


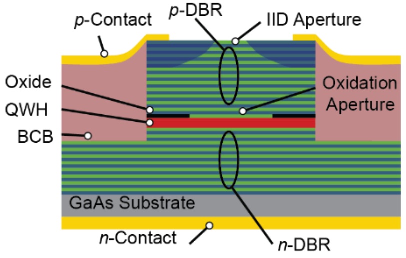
Research Areas [1]

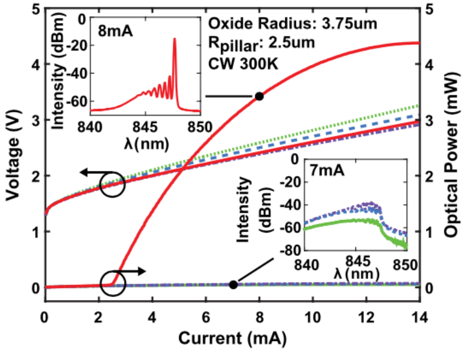
Heterogeneous Integration



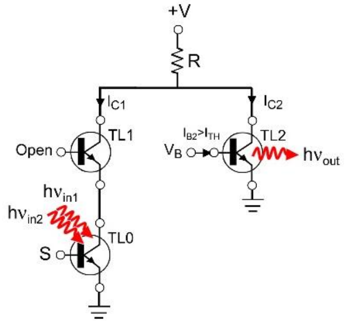
VCSEL Mode Control

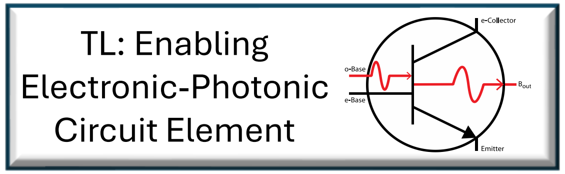


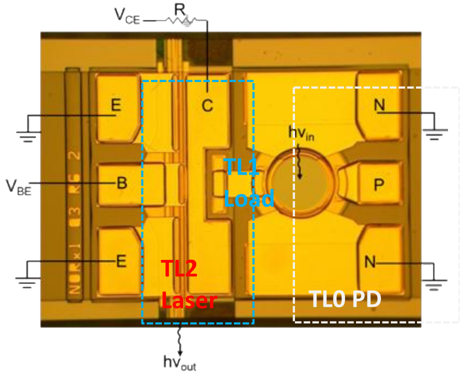




Transistor Laser Integration

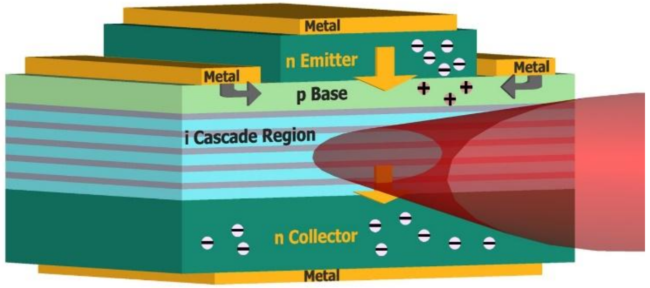


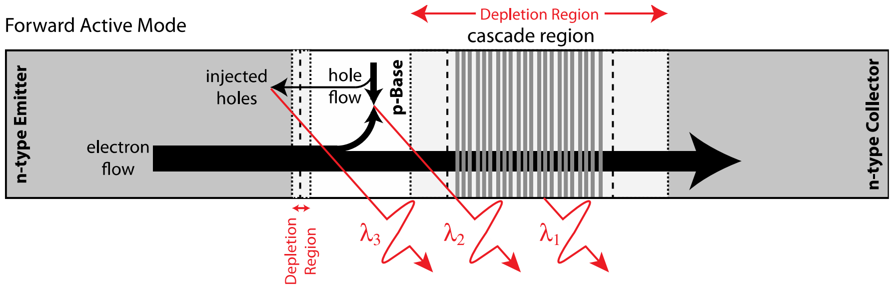


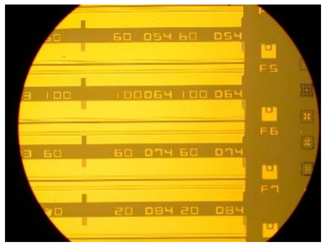


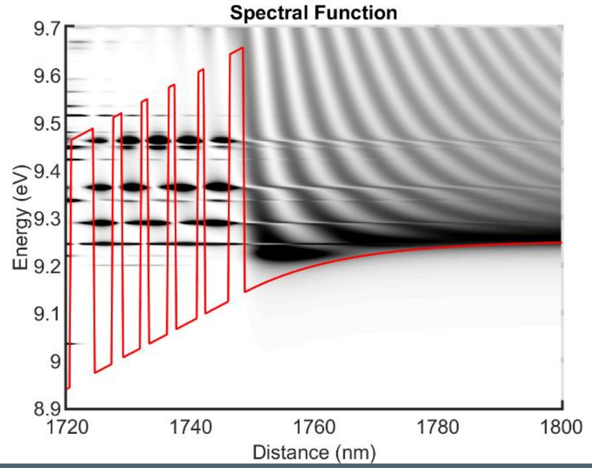
Research Areas [2]

Transistor-Injected QCL

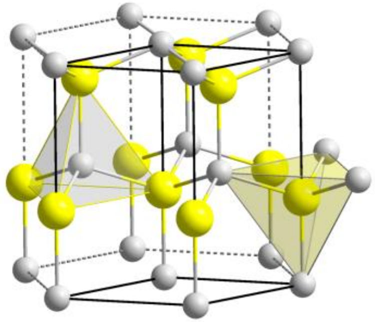




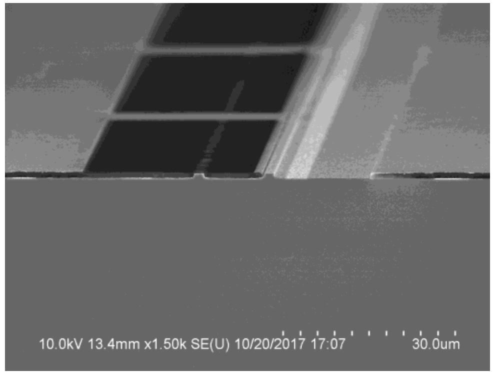




III-N Photonics



III-N MZMs & PICs

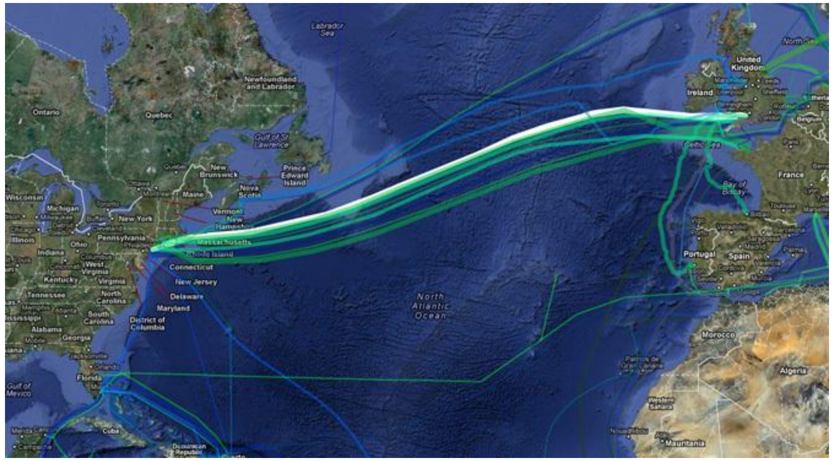


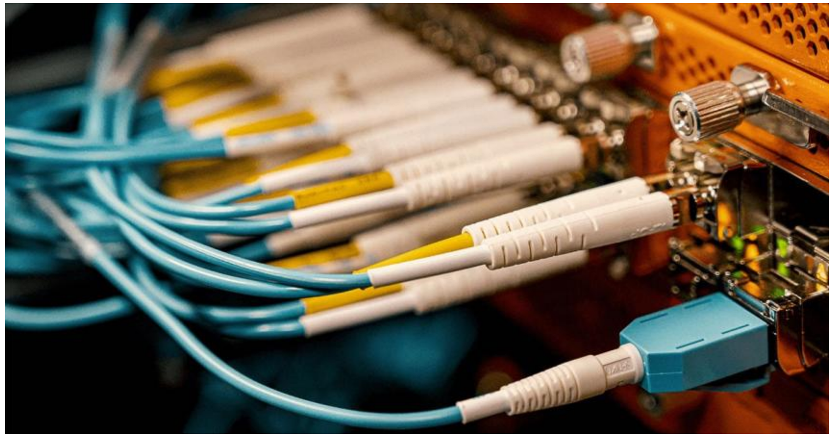
- Tunable Lasers, MZMs, Coherent Rx
- V-Controlled Polarization Rotators
- Quantum Computing

Motivation for Long-Wavelength VCSELs

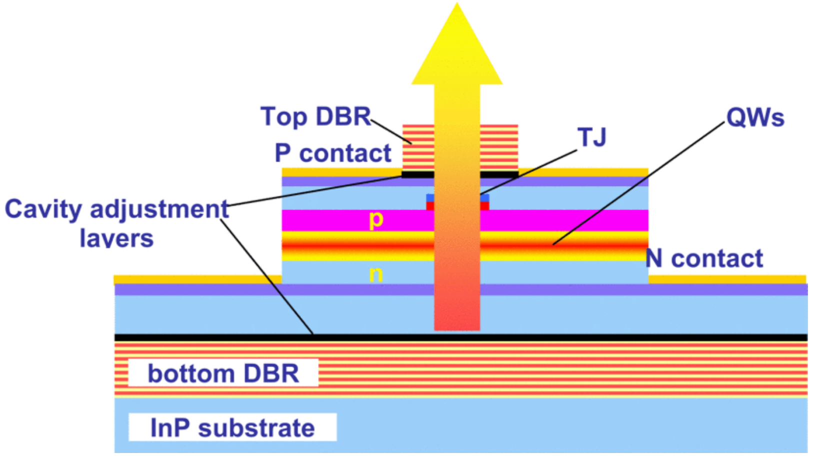
Long-Wavelength Emitters

- Demand for higher data communication traffic driven via AI/ML applications
- Eye safety concerns for NIR emitters in 3D-sensing and LiDAR
- Semiconductor DBRs expensive due to low refractive index difference, requiring many pairs
- Complicated alternatives with difficulty to scale





DBR Materials	Index Contrast $\Delta n=(n_H-n_L)$	No. of pairs for 99.9%	Stopband Width *	Total Thickness
InGaAsP/InP	0.178	65	51 nm	12.9 μm
$Al_{0.25}GaInAs/InP$	0.187	63	54 nm	12.3 μm
$Al_{0.25}GaAsSb/AlAsSb$	0.49	27	127 nm	5.2 μm
AlAs/GaAs	0.5	23	158 nm	4.8 μm
SiO2/TiO2	0.77	9	436 nm	3.3 μm
InP (λ/4n)/Air (λ/4n)	2.2	3	1379 nm	1.3 μm
InP (5λ/4n)/Air (λ/4n)	2.2	3	337 nm	2.4 μm



Problems with Long-Wavelength VCSELs

- DBRs
  - ➢Small index contrast (Δn) compared to 850 nm devices – more DBR pairs needed
  - ➢Each DBR pair is almost twice as thick – λ/4 thick layers are larger when λ is larger
  - ➢Includes quaternary layers (calibration/control)
- Overall Structure
  - ➢Control of electric field standing wave in gain region (confinement factor) and resulting impact on threshold modal gain
  - ➢Current injection
  - ➢Heat removal
- Impact
  - ➢Cost and yield

Presentation Outline

Introduction and Motivation

- Long-wavelength VCSEL Applications
- Issues, Limits, and Past attempts
- Novel Design

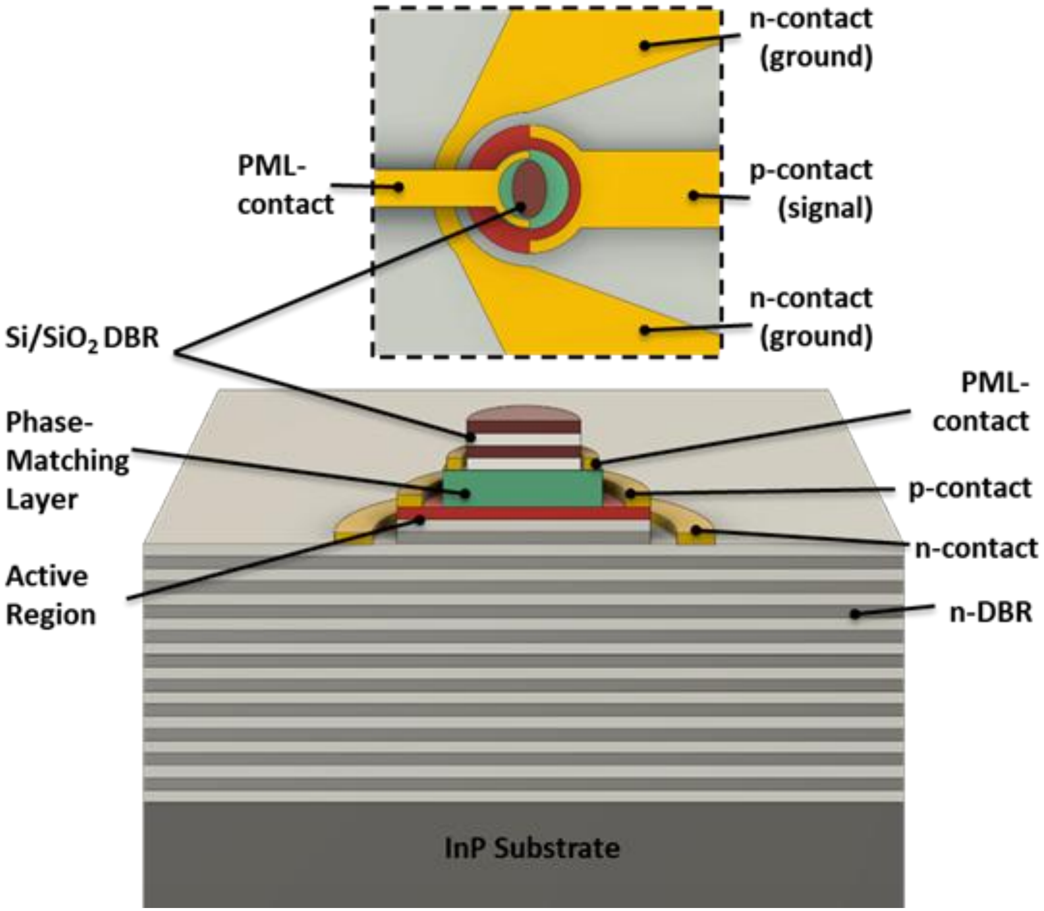
Long-Wavelength VCSEL Fundamentals

- Epitaxial Material Optimization
- Potential Structures & Fabrication

Phase-Matching Layer Progress

- Material Optimization
- Validation Experiment

Conclusion



Long-wavelength VCSEL structure with dielectric top DBR and phase-matching layer

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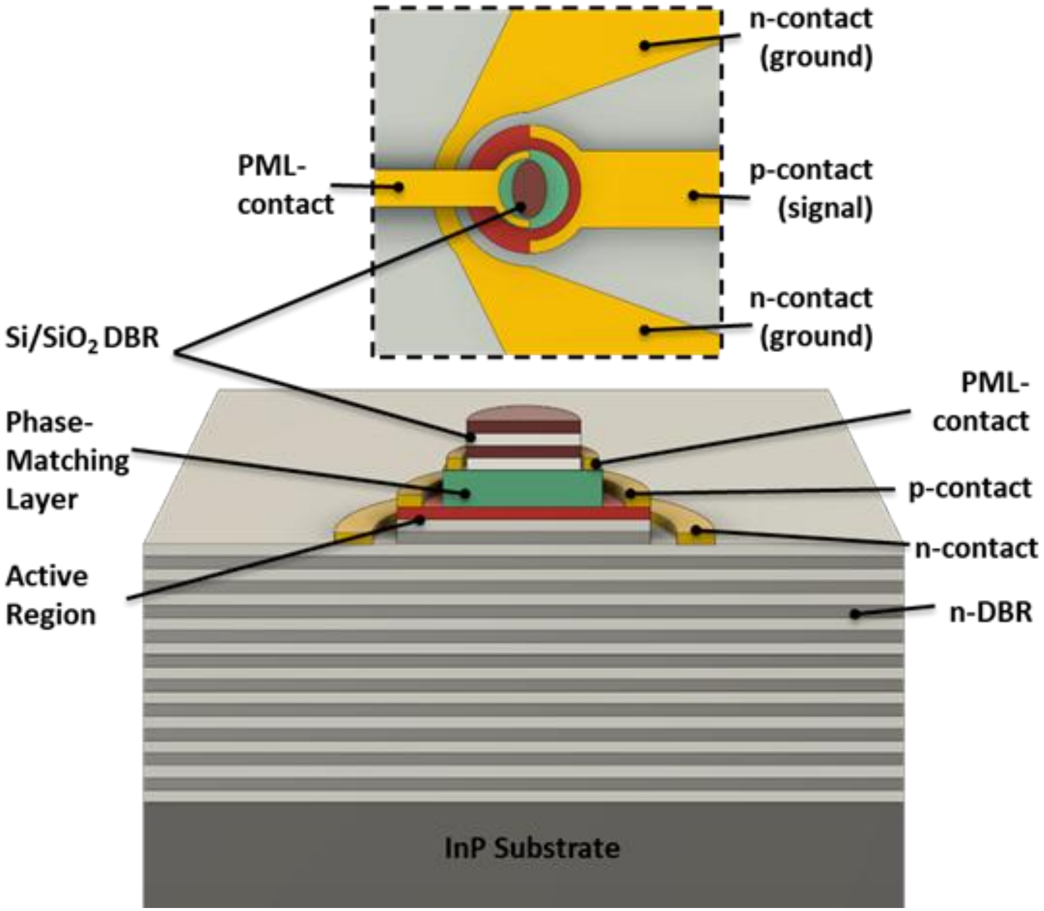


Long-wavelength VCSEL structure with dielectric top DBR and phase-matching layer

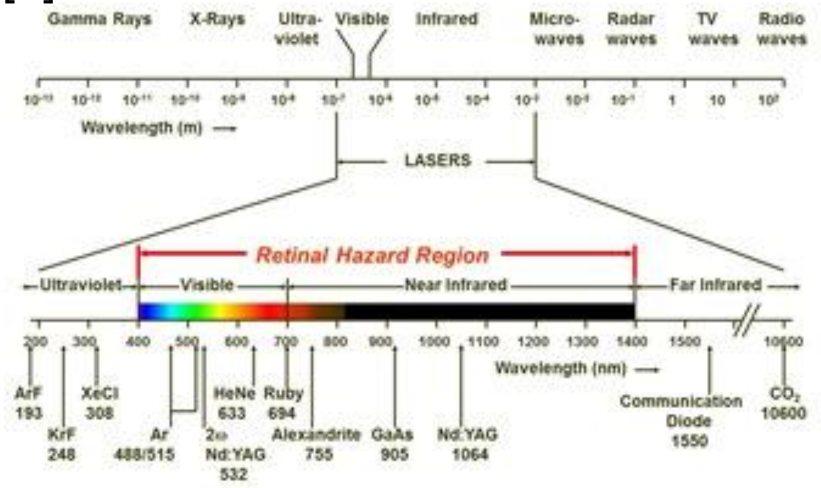
Dallesasse Group

Jason Flanagan

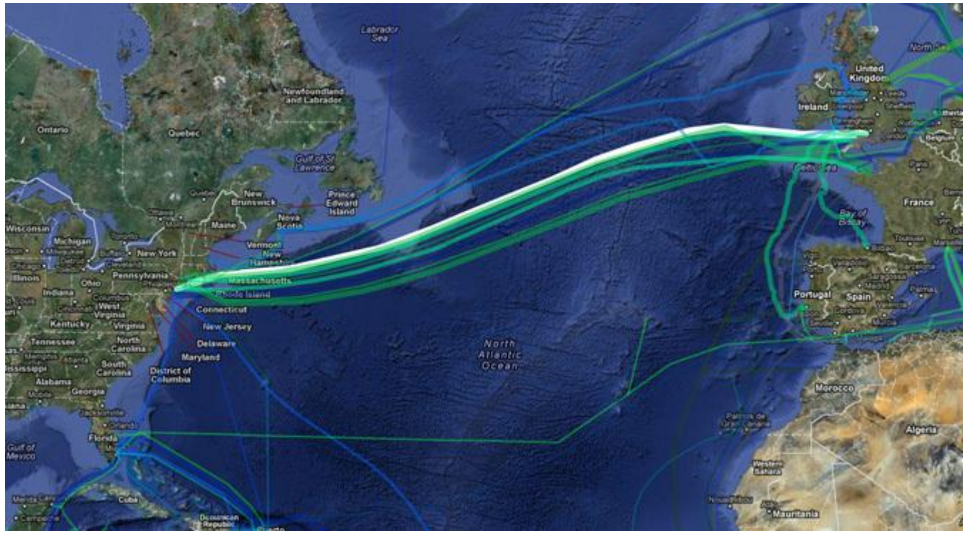
- University of Illinois Urbana-Champaign
- Electrical Engineering, M.S. (Expected 2026)
- B.S. Electrical Engineering from University of Illinois Urbana-Champaign (2024)
- VCSEL Design and Fabrication
- Focus on material deposition, optimization, and characterization alongside heterogeneous integration

Long-Wavelength Emitter Applications

[1]



[3]



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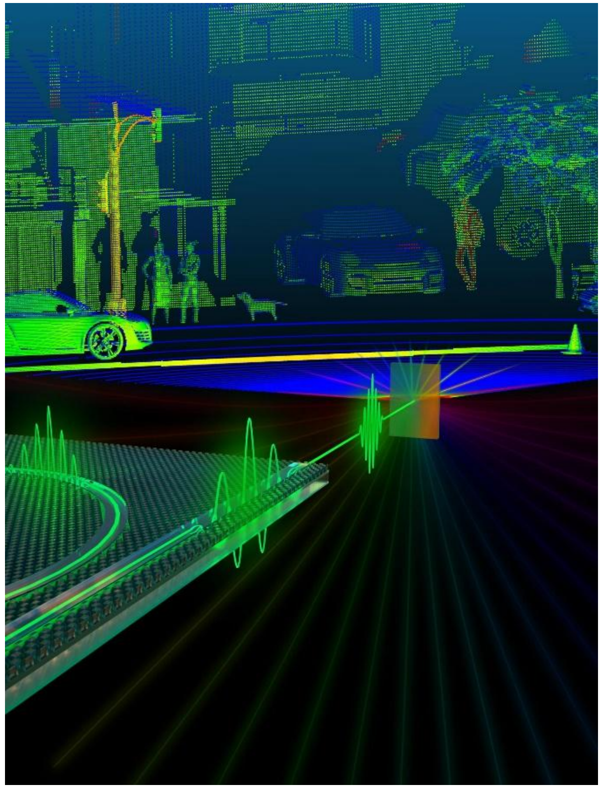

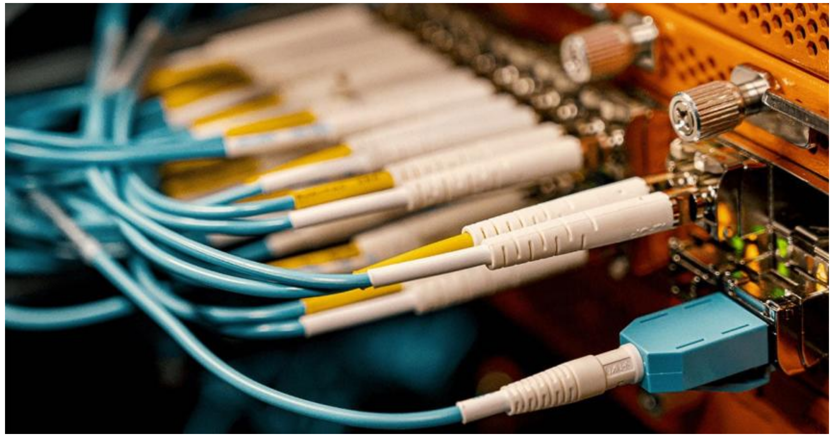

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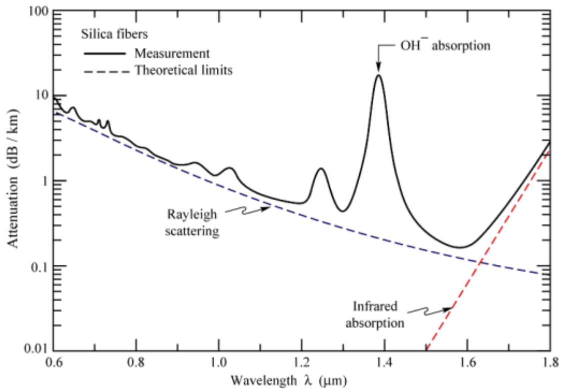


[4]

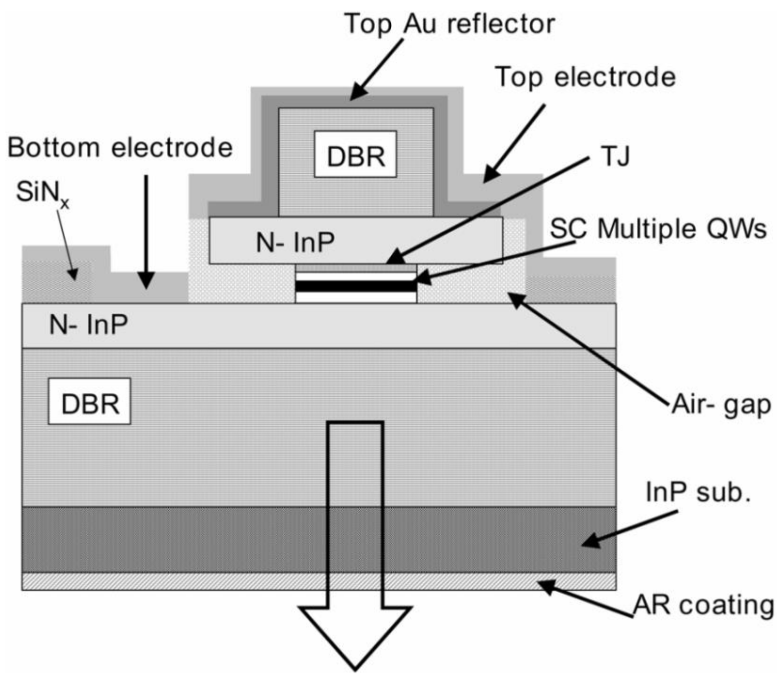
[5]

[7]

Long-Wavelength Approaches

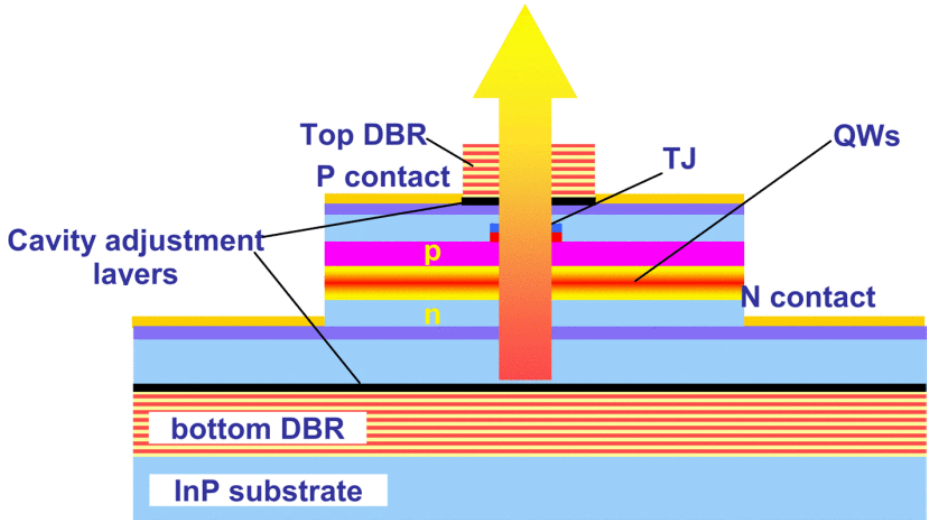
Monolithic Growth on InP [8]

- Achieved 37 dB side mode suppression ratio (SMSR), 2.5 mA threshold current and 1.6 mW output power
- 38 pairs on bottom DBR, 28 pairs on top



Wafer Fusion [9]

- Process to integrate AlGaAs/GaAs or top DBRs with direct bonding
  - 560°C for 30 minutes
- Output 5.5 mW of power at room temperature and 40 dB SMSR



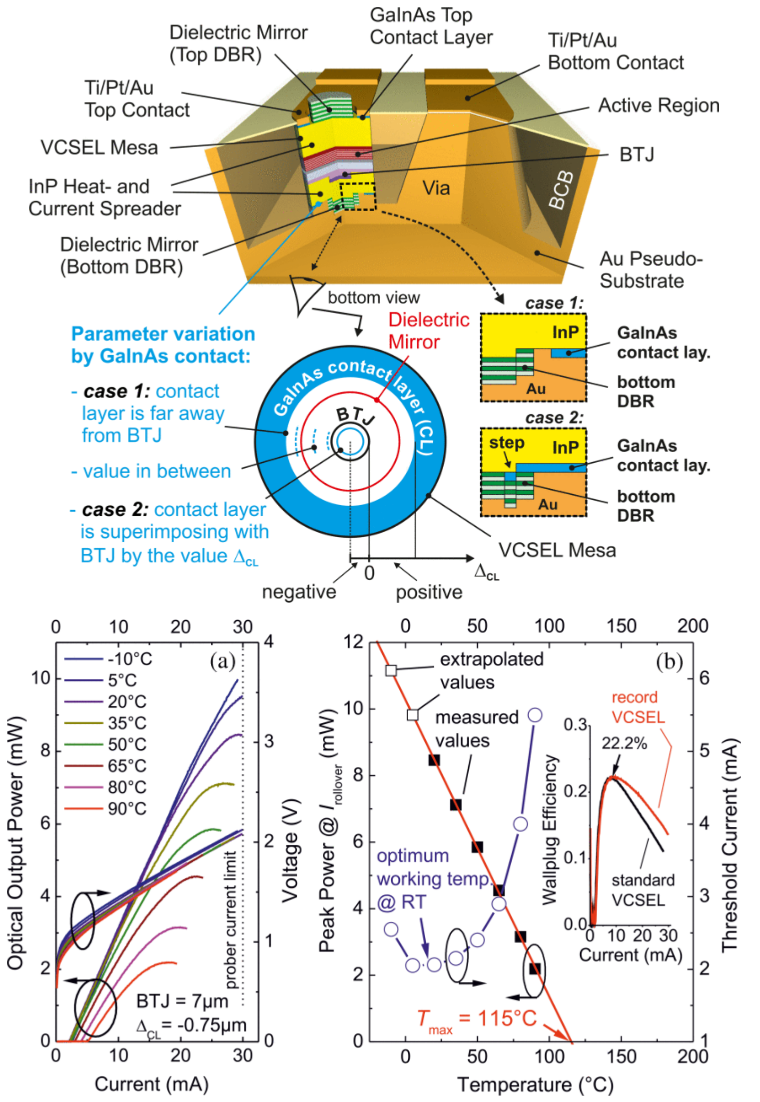
Long-Wavelength Approaches

Hybrid DBR [10]

- Device performance of 7.9 mW output power at room temperature and 2.2 mW at 90°C
- Used dielectric-, fluoride-, and sulfide-based mirrors
- Optimized for high power and not high-frequency

- GaInAs contact layer
  - Affects transverse mode profile

- Extensive simulation and testing to determine thermal effects for tuning large mode-gain offset



Current Issues and Limitations

Bragg Reflectors

- Difficult to lattice match to InP material system
- Shift towards dielectric DBRs/others
  - 2.5 pairs of CaF_2/ZnS give 99.85% reflectivity [12]
- Major thermal and bandwidth limitation

Thermal Properties

- Wafer fusion at high temperatures conflicts with thermal expansion mismatch
- Reliability of mode-gain offset

Fabrication

- Complex and expensive structures
- Difficulty with scaling and large-scale manufacturing
- Inconsistent deposition and processing techniques affect cavity resonance

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[11]

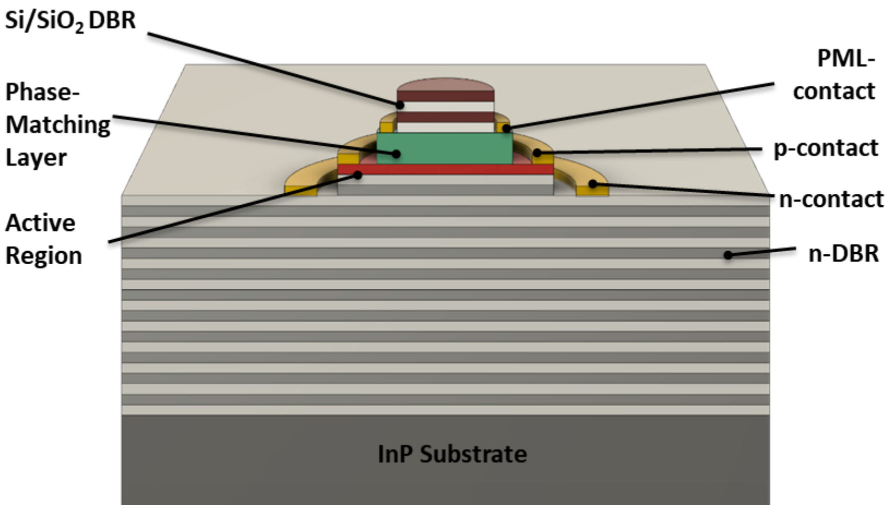
Novel Structure: Phase-Matching Layer

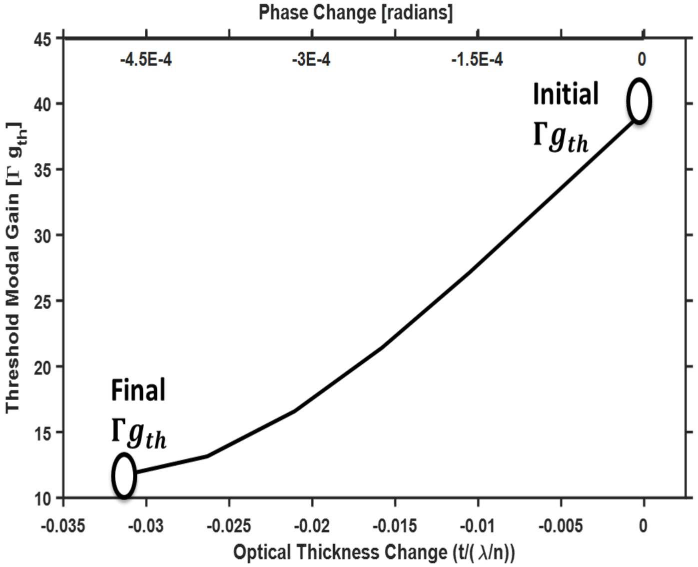
Objective

- Create a long wavelength VCSEL structure aimed at alleviating current issues
    - Thick and expensive DBR mirrors
    - Inconsistent growth and variation

Proposed Solution

- Replace top DBR with dielectric Si/SiO_2 mirror requiring only 3 pairs to achieve >97% mirror reflectivity
- Introduce voltage-controllable "phase-matching layer" to tune cavity standing wave pattern, optimizing performance, lowering threshold current, etc.
    - Piezo-electric, electro-optic material, e.g. PZT
- Current epitaxial material being refined
    - Depends on final structure and if further cost reduction measures are taken
    - Take into account thermal issues





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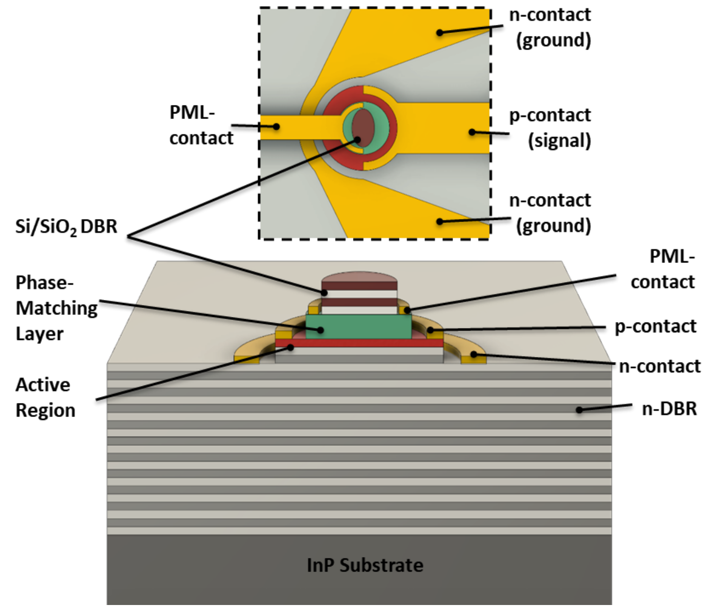

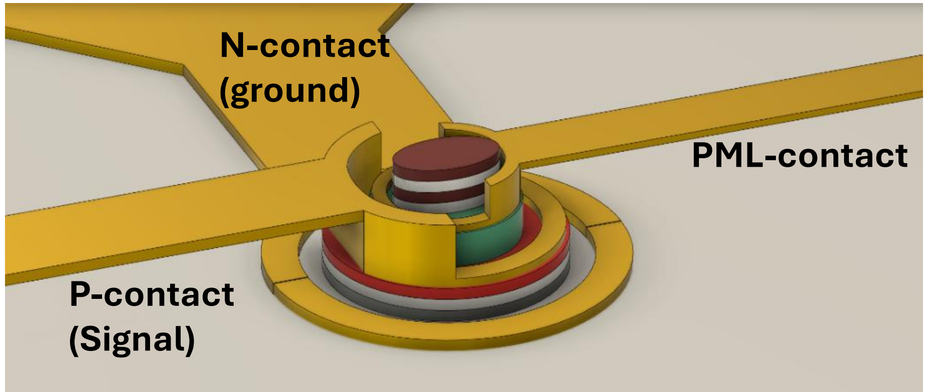

Block-Gift Grant Tasks & Milestones

Tasks in Year 1	Tasks in Year 2	Tasks in Year 3
○ 1.1: Design of 1550 nm VCSEL epitaxial structure ○ 1.2: TMM Simulations of full epitaxial structure including bottom DBR, PML, and dielectric top DBR ○ 1.3: Optimization of Phase-Matching Layer Structure ○ 1.4: Development of bonding process for PML material and epitaxial material ○ 1.5: Development of p-DBR deposition techniques ○ 1.6: Benchmarking of electro-optic performance for VCSEL epitaxial structure via electroluminescence measurements	○ 2.1: Deposition of dielectric DBR atop PML bonded to epitaxial material ○ 2.2: Mask design and layout of 1550 nm VCSELs ○ 2.3: Process flow and fabrication of 1550 nm VCSELs ○ 2.4: Benchmark of 1550 nm VCSELs for output power and spectral performance	○ 3.1: TMM simulations of single-mode, single-polarization VCSELs design ○ 3.2: Mask design and layout of single-mode, single-polarization VCSELs ○ 3.3: Process flow and fabrication of single-mode, single-polarization 1550 nm VCSELs ○ 3.4: Characterization of VCSELs for single-mode, single-polarization performance ○ 3.5: Characterization of modulation response in 1550 nm VCSELs

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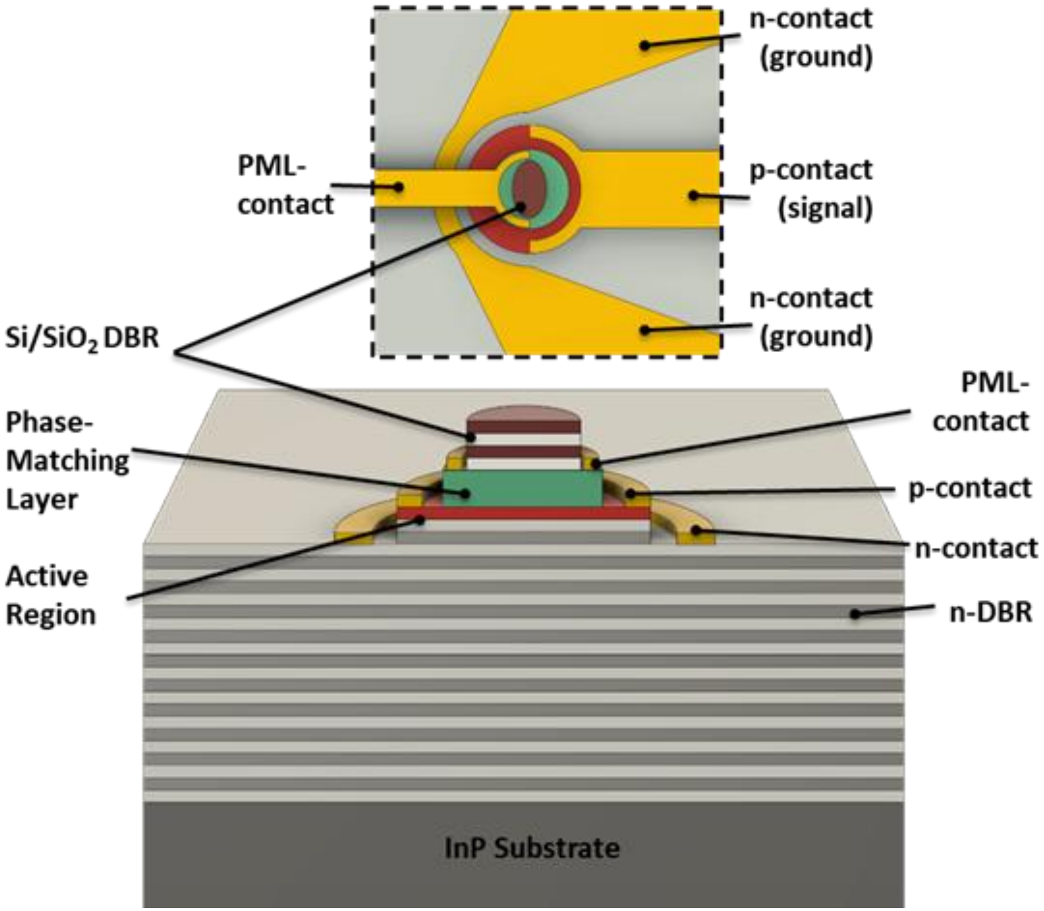


Long-wavelength VCSEL structure with dielectric top DBR and phase-matching layer

Dallesasse Group

Student Bio: Kevin Pikul, Ph.D.

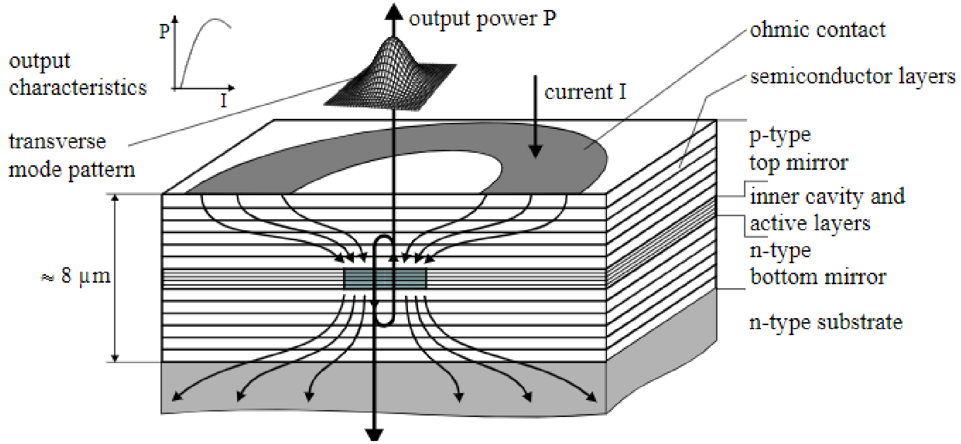
- UIUC, ECE, Professor Dallesasse, Ph.D.
- Undergrad: Engineering Physics, JJC then UIUC
- Research: Photonics, VCSELs
- Skills: Single-mode, single-polarization VCSEL design and simulation, semiconductor fabrication, VCSEL and material characterization, presentation, management
- Awards: Best student presentation at CS MANTECH, Editors Pick for APL publication
- 1st first-author publication just accepted (aiming for one more), 3 co-author
- 5 mini-conferences, 4 CS MANTECH
- Golfing, fishing, hiking, cooking, gym & nutrition
- Upcoming career plans: Senior Process Integration Engineer at Coherent Corp.

VCSEL Device Structure

Vertical-Cavity Surface-Emitting Lasers

- VCSELs employ distributed Bragg reflectors (DBR) for highly reflective mirrors that surround quantum-wells used as the active region
- Modern VCSELs utilize a current-confinement aperture to significantly reduce thresholds and optical modes
- Small footprint and vertically emitting device that operates at high quantum efficiency and can readily be formed into arrays

Cross-sectional Schematic of an Oxide-Confined VCSEL

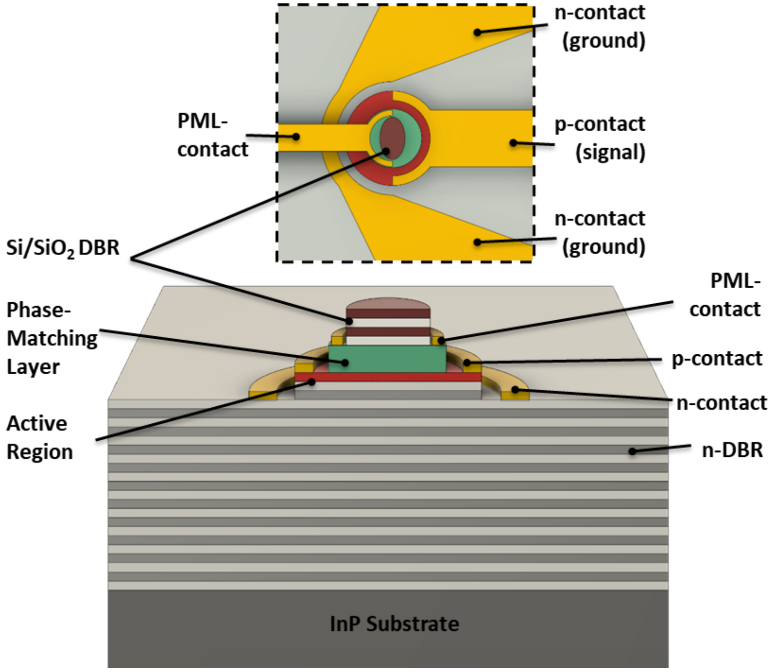


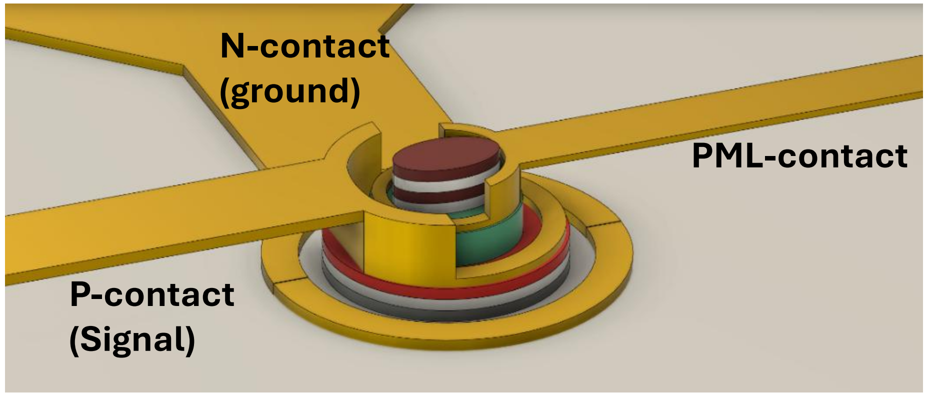
Michalzik, Rainer. "VCSEL fundamentals." *VCSELs*. Springer, Berlin, Heidelberg, 2013. 19-75.

Epitaxial Material Considerations and Structure Fabrication

- Different epitaxial materials will weigh cost and ease of fabrication
  - Original epitaxial material with semiconductor bottom DBR proved prohibitive from cost perspective
  - Required redesign to alleviate cost

- Different structures will require different fabrication processes
  - Ease of fabrication with semiconductor bottom DBR
  - Further redesigns will require a more intensive fabrication process with bonding and careful alignment steps



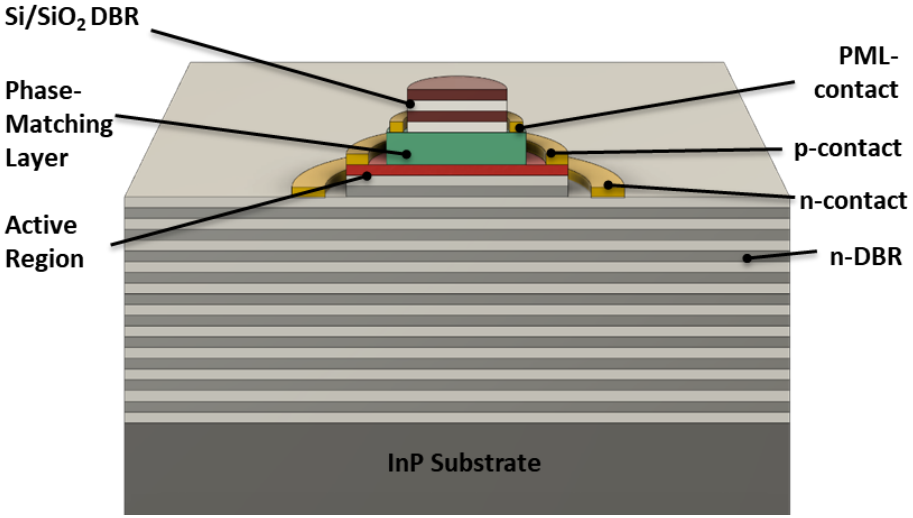


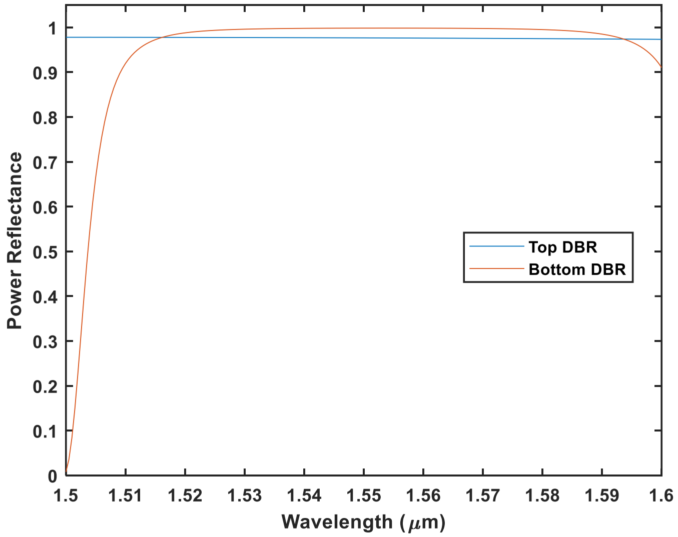
Structure 1 – Semiconductor DBR

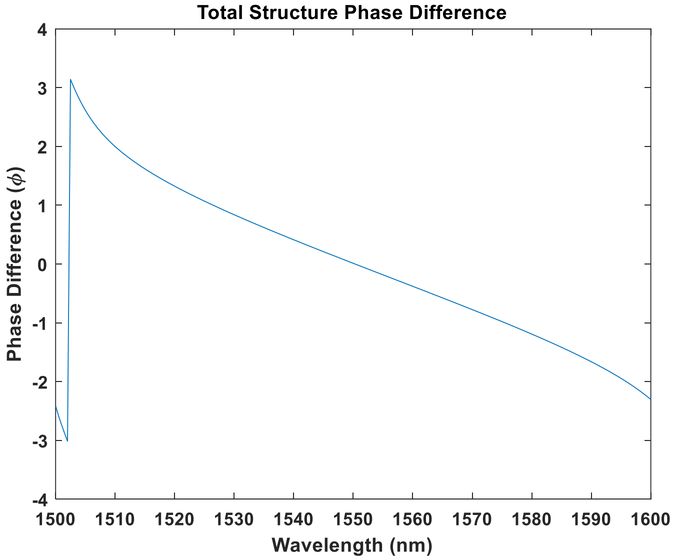
Simulated Structure

- InP substrate
- 44 bottom DBR pairs
  - $InP/In_{0.53}Al_{0.08}Ga_{0.39}As$
- Active Region
  - 5 wells:
  - $In_{0.52}Al_{0.24}Ga_{0.24}As$ barriers
  - $In_{0.53}Ga_{0.47}As$ wells
- Top DBR:
  - 1 semiconductor DBR pair
  - Oxide Layer
  - Phase-Matching Layer
  - High-doped InP Cap
  - 3 top Si/SiO_2 pairs

Threshold Modal Gain: **78.6 cm^{-1}**







Shin, J-H., Yoo, B.S., Han, W.S., Kwon, O.K., Ju, Y.G., and Lee, J.H. "CW operation and threshold characteristics of all-monolithic InAlGaAs 1.55-μm VCSELs grown by MOCVD." *IEEE Photonics Technology Letters* 14.8 (2002): 1031-1033.

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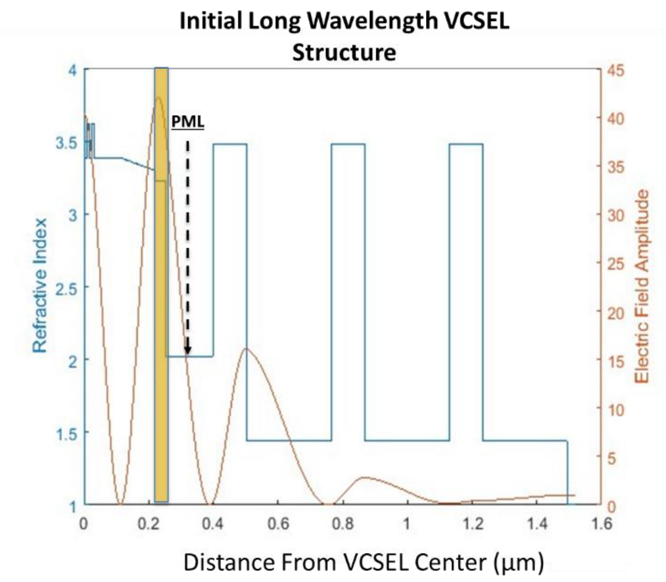
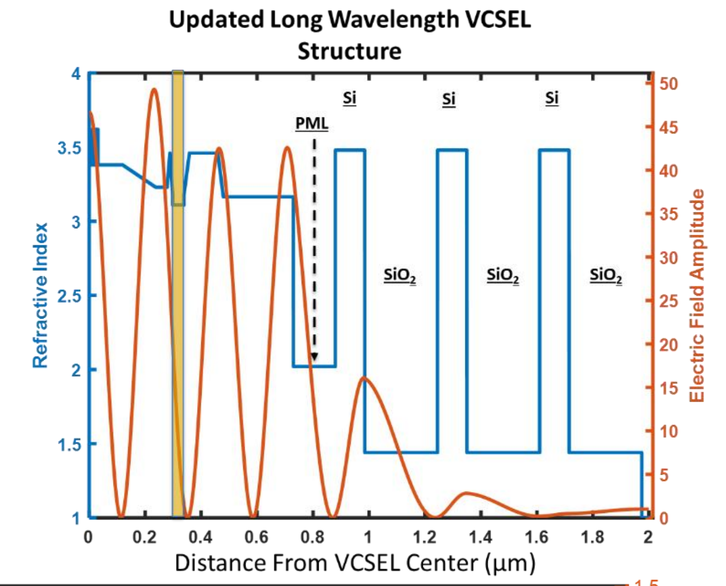
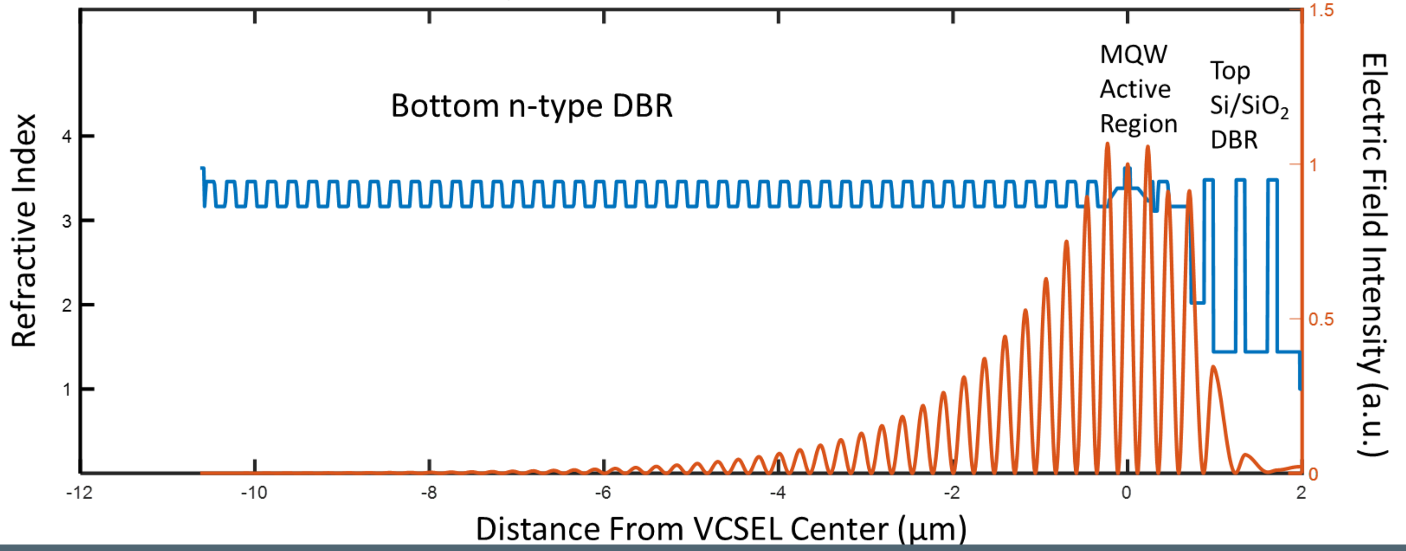
  - 3 top Si/SiO_2 pairs

Threshold Modal Gain: **78.6 cm^{-1}**

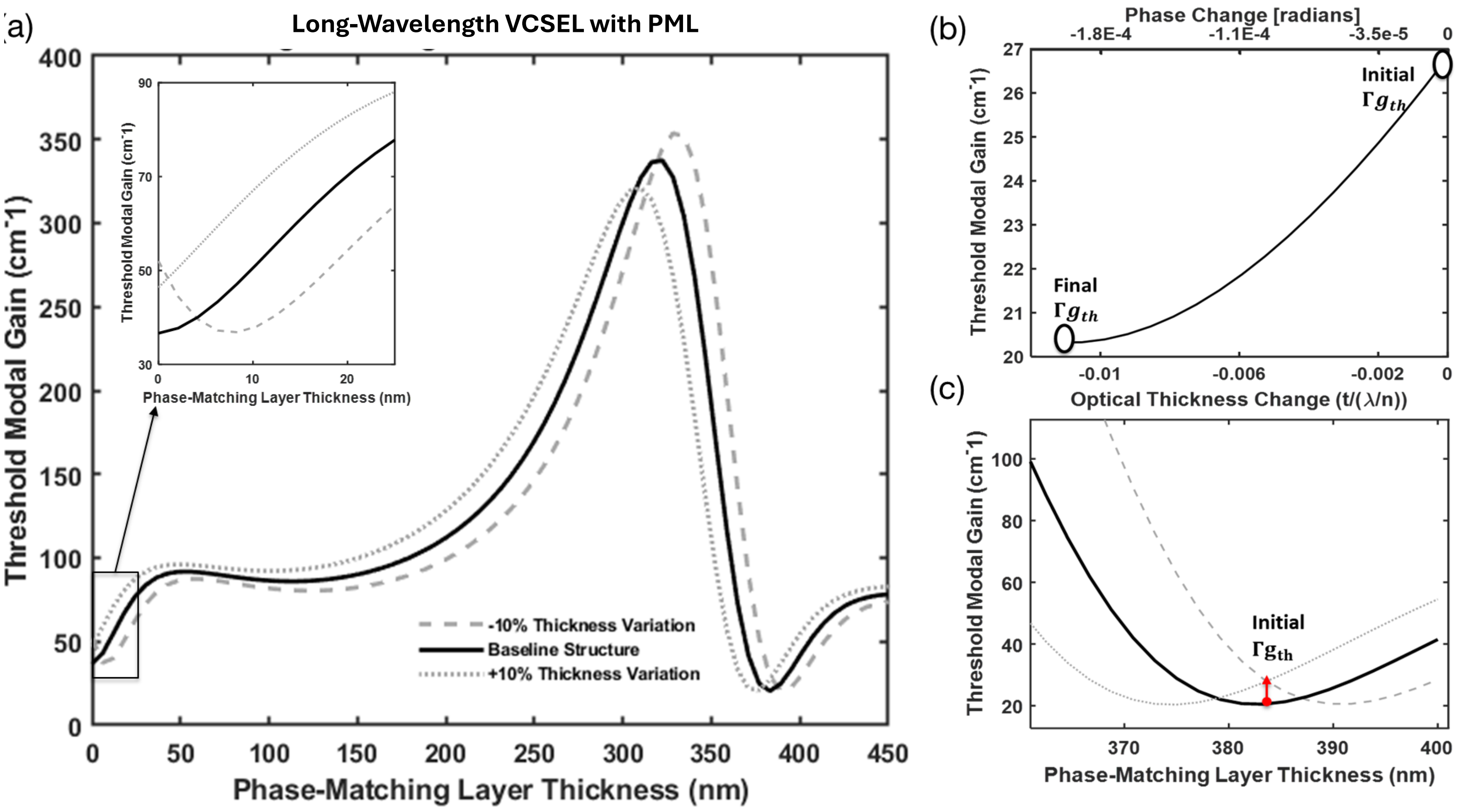






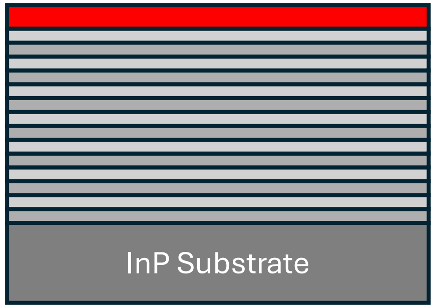
Structure 1 Tunability

- Standing-wave pattern overlap with active region can be tuned via voltage bias across phase-matching layer
- With a ± 10% variation in layer thickness due to nonuniformity, threshold modal gain can be tuned to a minimal value
- Validation/optimization of phase-matching layer performance is vital for proper operation and tunability

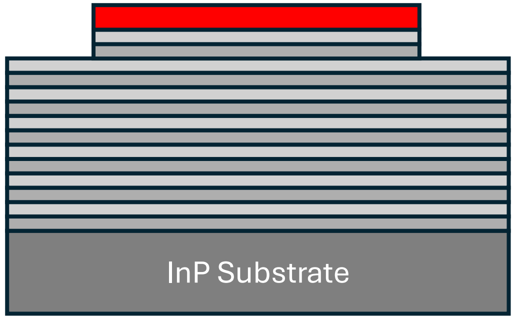


Long-Wavelength VCSELs-Fabrication 1

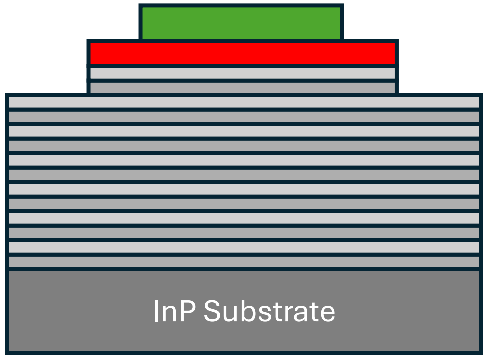
1. Grow Bottom DBR and Active Region



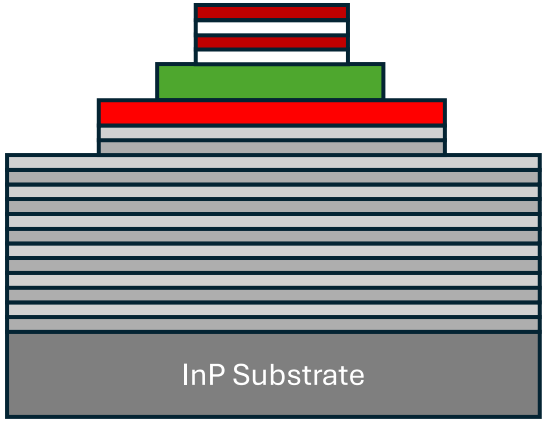
2. Etch Mesas



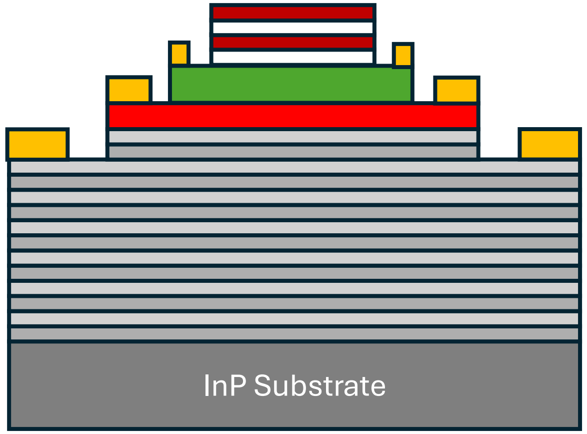
3. Deposit/bond PML



4. Deposit top DBR



5. Metallization

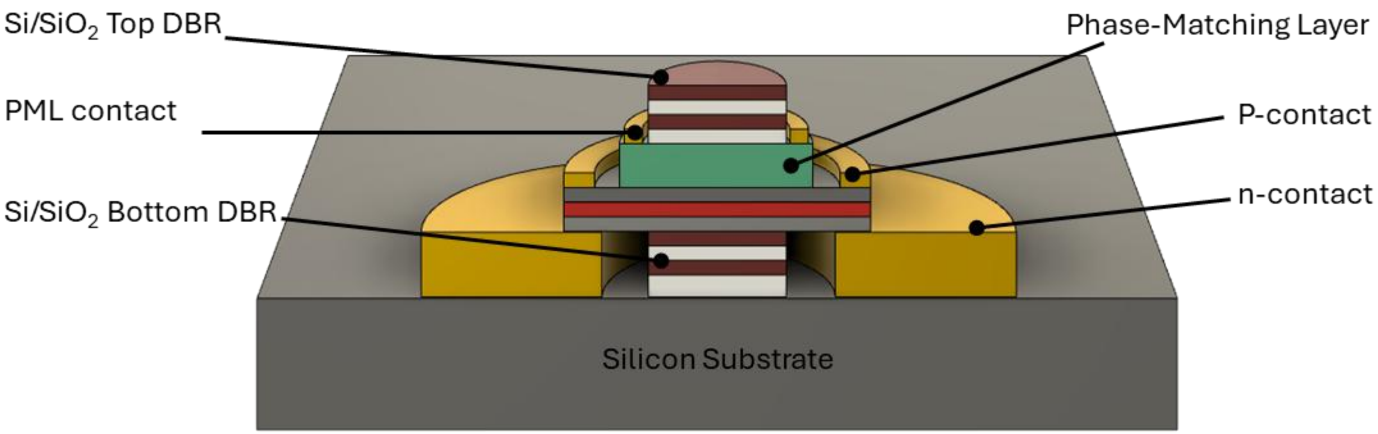


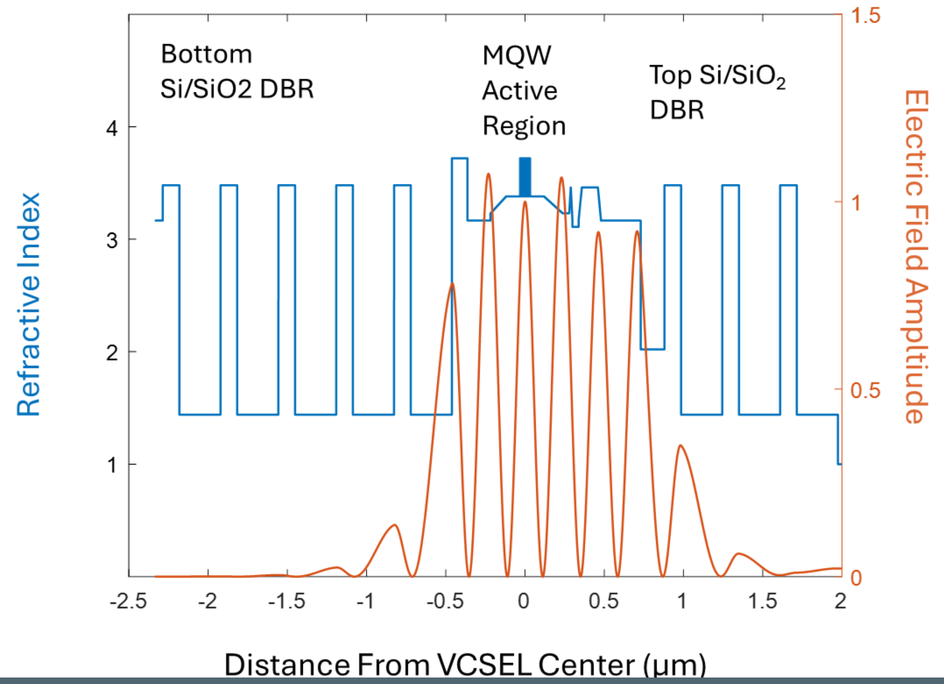
Structure 2 – Dielectric DBR

Simulated Structure

- InP substrate
- Bottom DBR: Si/SiO_2
- $In_{0.53}Ga_{0.47}As$ Etch Stop
- Active Region
  - 5 wells:
  - $In_{0.52}Al_{0.24}Ga_{0.24}As$ barriers
  - $In_{0.53}Ga_{0.47}As$ wells
- Top DBR:
  - 1 semiconductor DBR pair
  - Oxide Layer
  - Phase-Matching Layer (AlN is simulated here)
  - High-doped InP Cap
  - 3 top Si/SiO_2 pairs

Threshold Modal Gain: **139 cm^{-1}**





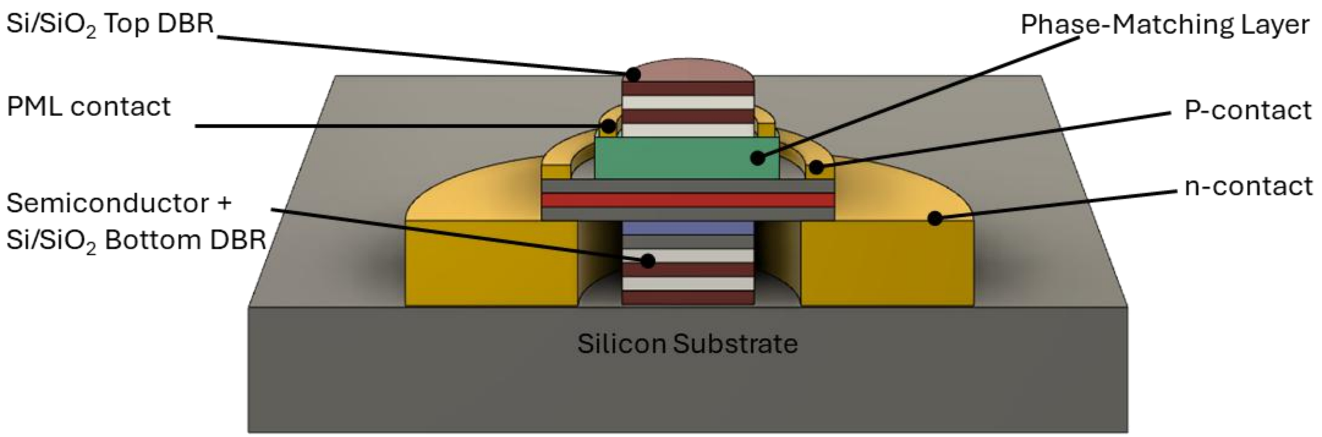
Structure 3 – Hybrid DBR

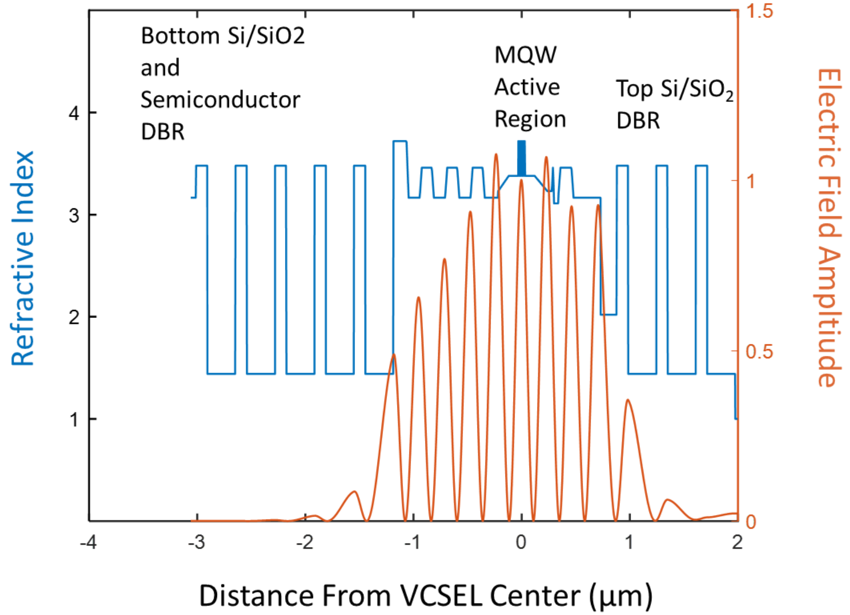
Simulated Structure

- InP substrate
- Bottom DBR:
  - Si/SiO_2,
  - $In_{0.53}Ga_{0.47}As$ Etch Stop
  - 3 $InP/In_{0.53}Al_{0.08}Ga_{0.39}As$ pairs
- Active Region
  - 5 wells:
  - $In_{0.52}Al_{0.24}Ga_{0.24}As$ barriers
  - $In_{0.53}Ga_{0.47}As$ wells
- Top DBR:
  - ~1 semiconductor DBR pair
  - Oxide Layer
  - Phase-Matching Layer (AlN is simulated here)
  - High-doped InP Cap
  - 3 top Si/SiO_2 pairs

Threshold Modal Gain: **103 cm^{-1}**

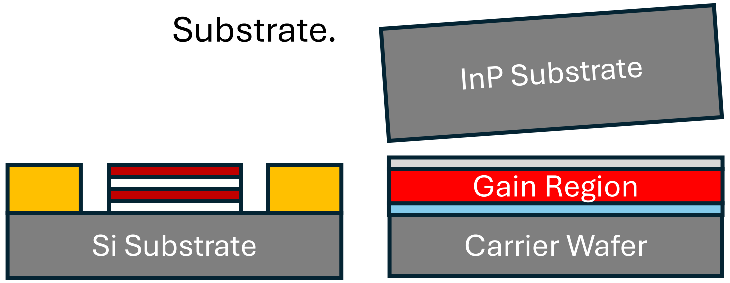
- With additional pairs, modal gain decreases further



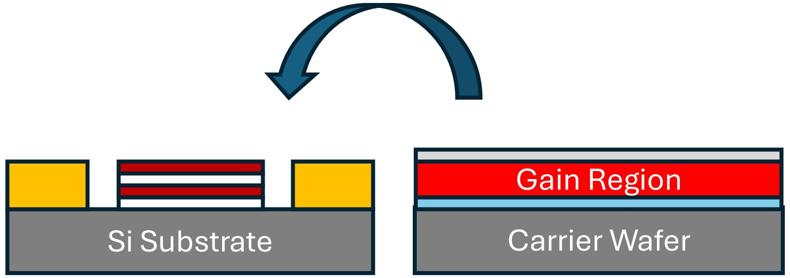


Long-Wavelength VCSELs-Fabrication 2

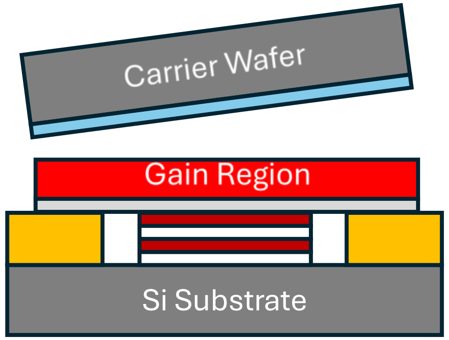
1. Pattern Si Substrate with bottom metal and bottom DBR. Bonding gain region epi to carrier wafer. Remove InP Substrate.



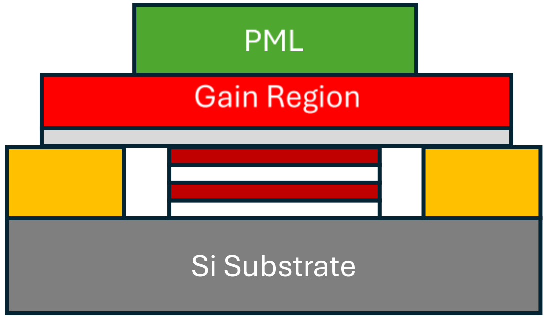
2. Bond gain region to bottom DBR



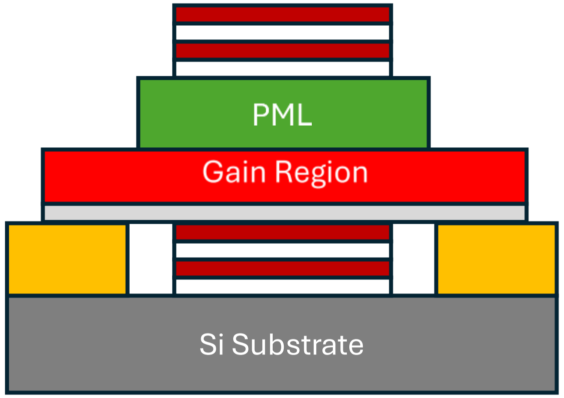
3. Remove the carrier wafer



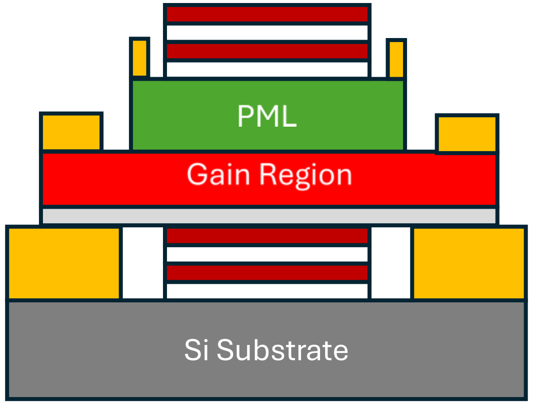
4. Deposit/bond PML



5. Deposit top DBR



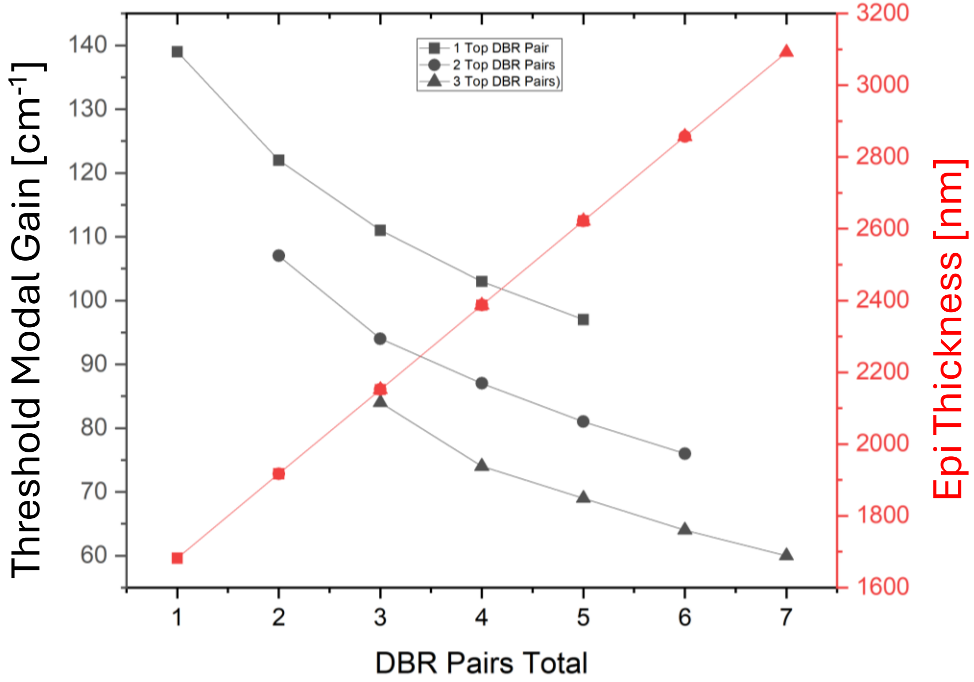
6. Metallization



Further Epi Optimizations

		Bottom Pairs				
	Threshold Gain (cm^{-1})	0	1	2	3	4
Top Pairs	1	139.0	122.5	111.6	103.1	97.2
	2	107.6	94.8	87.2	81.1	76.9
	3	84.0	74.7	69.3	64.7	60.2

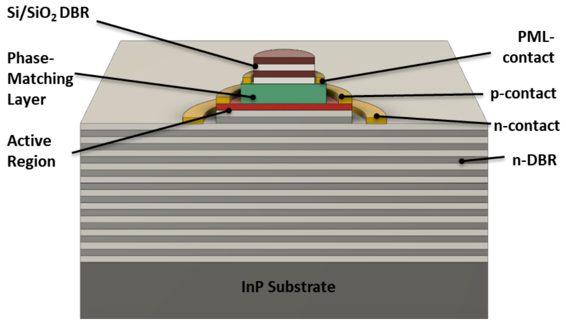
		Bottom Pairs				
	Thickness (nm)	0	1	2	3	4
Top Pairs	1	1682	1917	2152	2387	2622
	2	1917	2152	2387	2622	2857
	3	2152	2387	2622	2857	3092



- Further combinations of dielectric/semiconductor DBR pairs in bottom DBR being explored
  - Balance thermal heat dissipation, cost, and fabrication
- As number of semiconductor pairs go up, threshold modal gain decreases but cost of growth is driven up
- Needed to compromise on structure but alleviated additional issue regarding total thickness and

Fabrication of VCSEL Structures

V1



Fabrication

- Most straightforward
- Standard oxide-confined VCSEL process flow with additional top DBR deposition and 3 top contacts

Cost

- Most expensive
- ~40 bottom DBR pairs

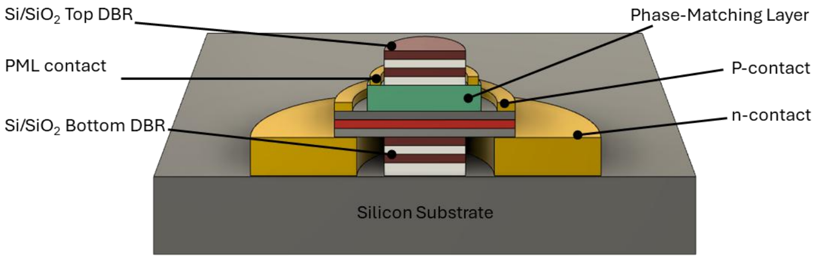
Performance

- Most optimal
- Lowest threshold modal gain of 3 options (78.6 cm^{-1})

Epi Thickness

- Thickness > 11 µm

V2



Fabrication

- Most difficult
- Multiple bonding steps with careful alignment enabled via bonding tool

Cost

- Least expensive
- Only substrate, etch stop, and active region layers are grown with dielectric mirrors grown via e-beam evap.

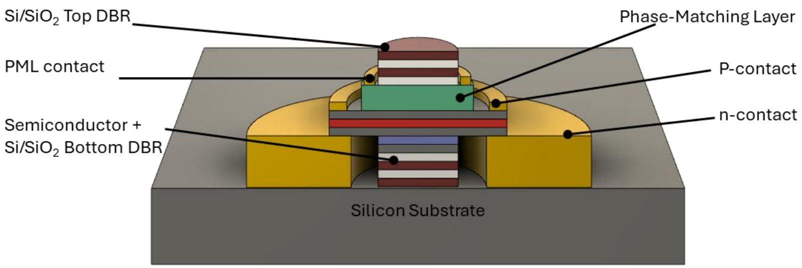
Performance

- Least optimal
- Highest threshold modal gain (106 cm^{-1})

Epi Thickness

- Thickness < 1 µm

V3



Fabrication

- Most difficult
- Multiple bonding steps with careful alignment enabled via bonding tool

Cost

- Less expensive
- Only few additional DBR pairs are grown

Performance

- More optimal
- Lower threshold modal gain than dielectric only DBRs (~100 cm^{-1})

Epi Thickness

- Thickness ~2-3 µm

Presentation Outline

Introduction and Motivation

- Long-wavelength VCSEL Applications
- Issues, Limits, and Past attempts
- Novel Design

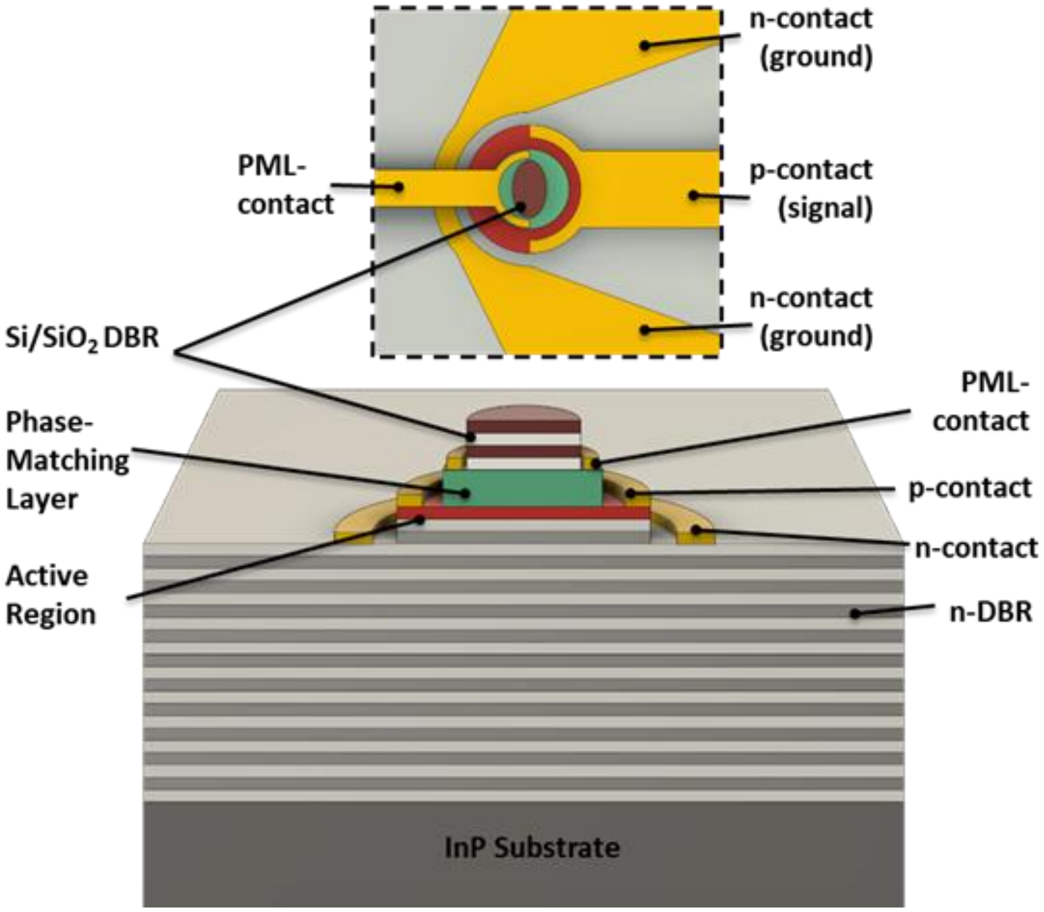
Long-Wavelength VCSEL Fundamentals

- Epitaxial Material Optimization
- Potential Structures & Fabrication

Phase-Matching Layer Progress

- Material Optimization
- Validation Experiment

Conclusion



Long-wavelength VCSEL structure with dielectric top DBR and phase-matching layer

Dallesasse Group

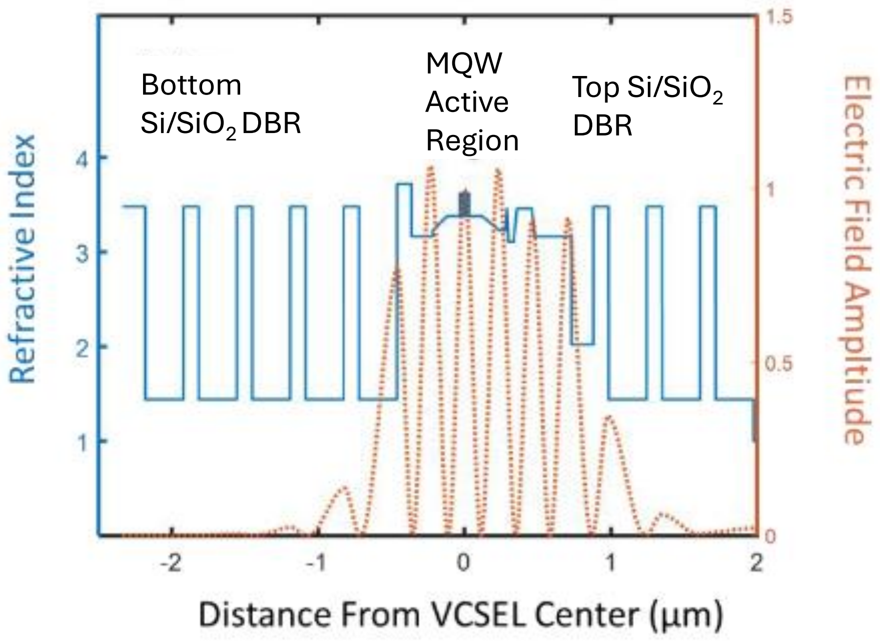
Emily Becher

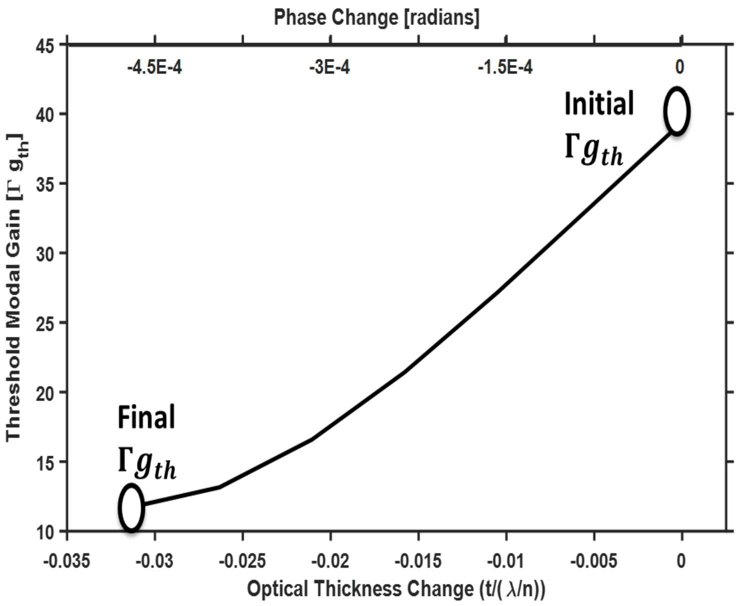
- University of Illinois Urbana Champaign
- Electrical Engineering, PhD
- B.S. Electrical Engineering from Oregon State University (2024)
  - Minors in Computer Science and Mathematics
- Researching semiconductor lasers and photonic devices
  - Focusing on LW VCSEL fabrication and characterization
- Current work involves numerical modeling of device structures, III-V device fabrication, and characterization of electrical and optical device performance
- Promise of Excellence Fellowship (2024)

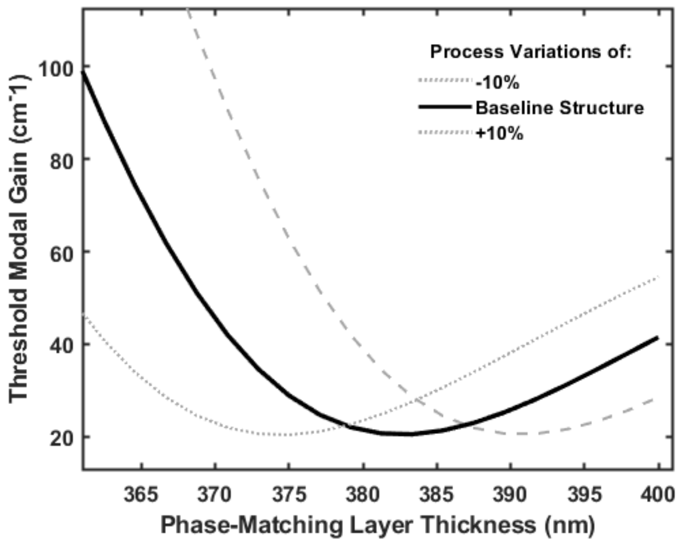
Phase-Matching Layer Motivation

Phase-Matching Layer Motivation

- Tunable optical cavity length can account for non-uniformity in growth between and within wafers
- Can tune the optical thickness to maximize the electric field standing wave overlap with the active region thus minimizing the threshold modal gain and threshold current







Phase-Matching Layer Materials

Material	Refractive Index	Electro-optic Coefficient	Piezo-electric Coefficient
Lead Zirconate Titanate (PZT)	2.43	300 pm/V	350 pm/V
Scandium-doped Aluminum Nitride	2.02	3 pm/V	20 pm/V
Lithium Niobate	2.21	30 pm/V	20 pm/V
Silicon	3.43	Thermo-optic coefficient: $1.9 * 10^{-4} K^{-1}$	

PZT Phase-Matching Layer

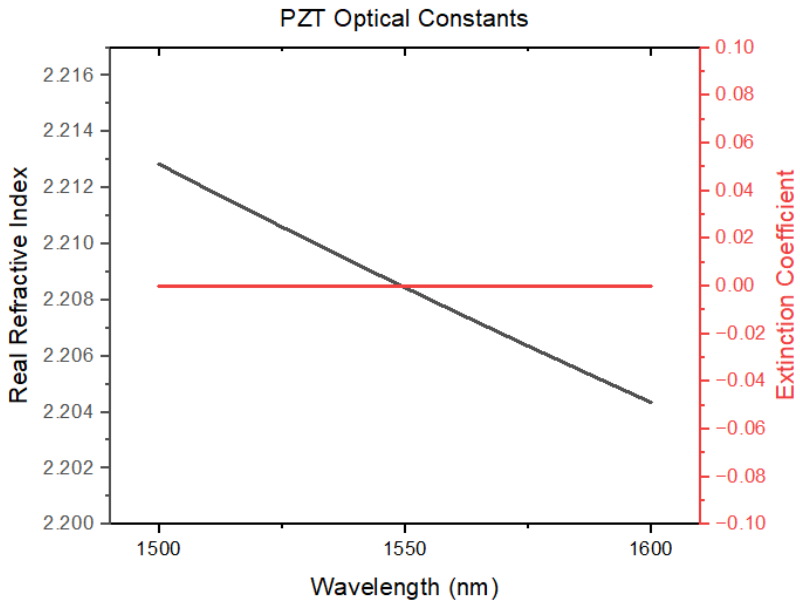
Chosen Material: PZT

- Highest potential for optical path length change based on electro-optic and piezo-electric coefficients
- Had access to a PZT sputtering target
- No measured absorption at 1550 nm
    - Critical for optimal laser operation and low threshold conditions

Design Considerations

- Piezo-electric properties are much better when in perovskite phase
    - Requires high temperature annealing
- Based on simulations, the PZT layer thickness will be ~150 nm

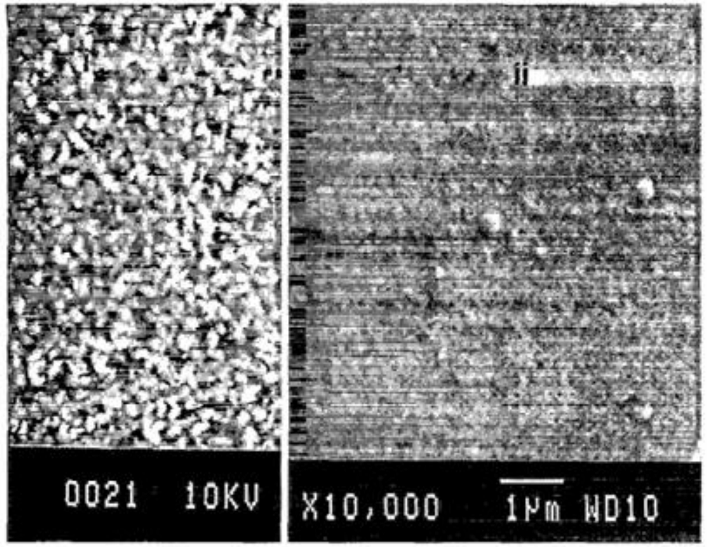
Material	Refractive Index	Electro-optic Coefficient	Piezo-electric Coefficient
Lead Zirconate Titanate (PZT)	2.43	300 pm/V	350 pm/V



PZT Optimization

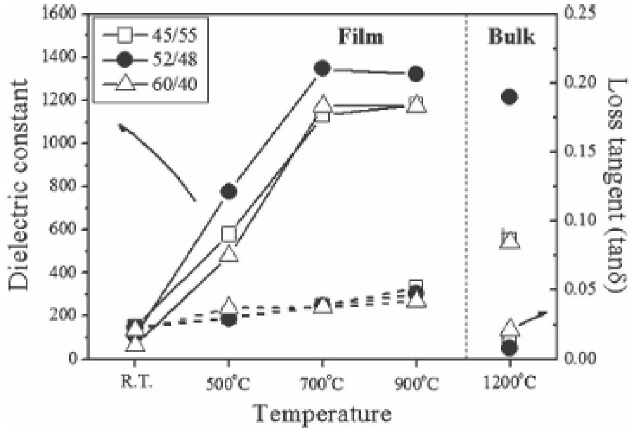
Next Steps to Optimize the PZT Film

- Anneal film above at least 500°C to ensure perovskite phase
- Rapid thermal annealing has been shown to inhibit grain growth which increases the dielectric coefficient
- Heat substrate during PZT sputtering to create denser film and perovskite phase
- Identify contacts that form Schottky barriers to minimize current through the PML
- Increase the resistivity of the PZT film to minimize current through the PML



[13]

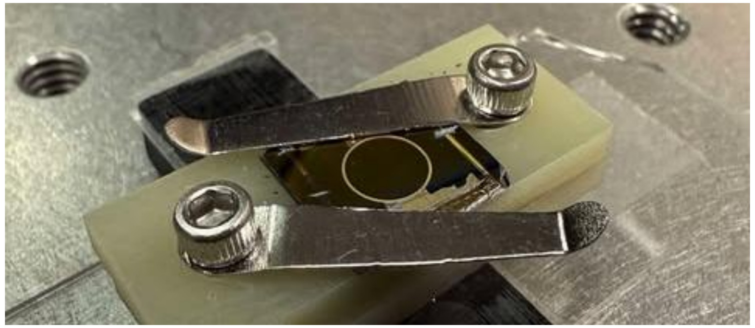
Surface morphology of PZT films as sputtered (left) and after 600°C anneal (right)

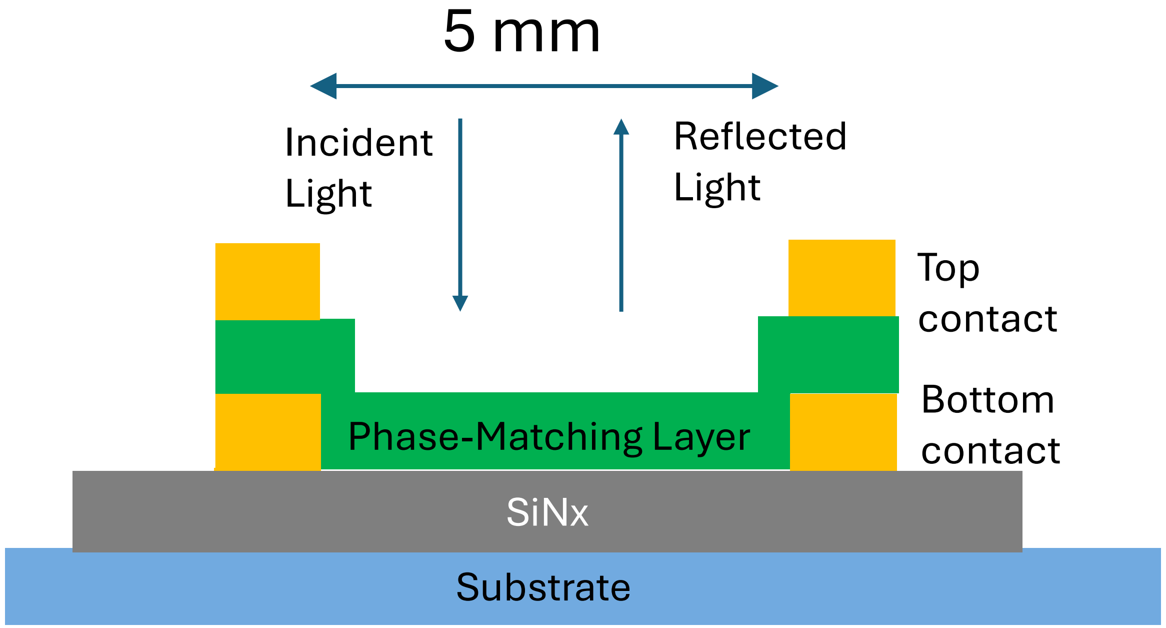


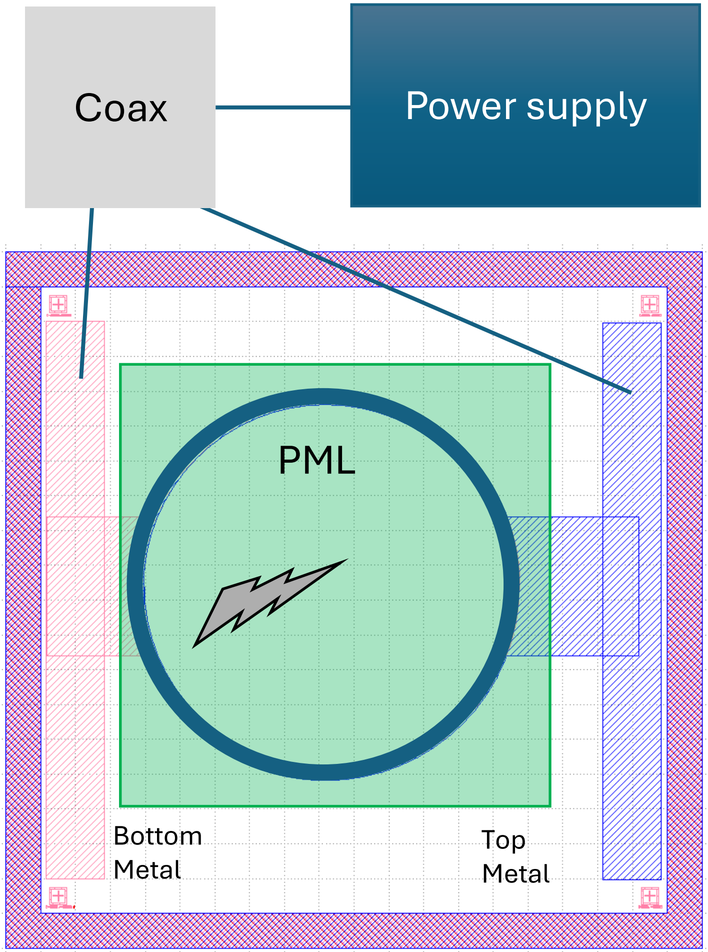
[14]

PML Validation Experiment

Validation Experiment
- Utilizing a spectrophotometer and fabricated sample seen here, validation of PZT as phase-matching layer can occur
- Incident light beam shined onto metal ring on sample and sample is biased at different voltages (0-3 V)
- Reflected light is measured
  - Any change in PZT optical thickness would register as change in reflectivity of the sample



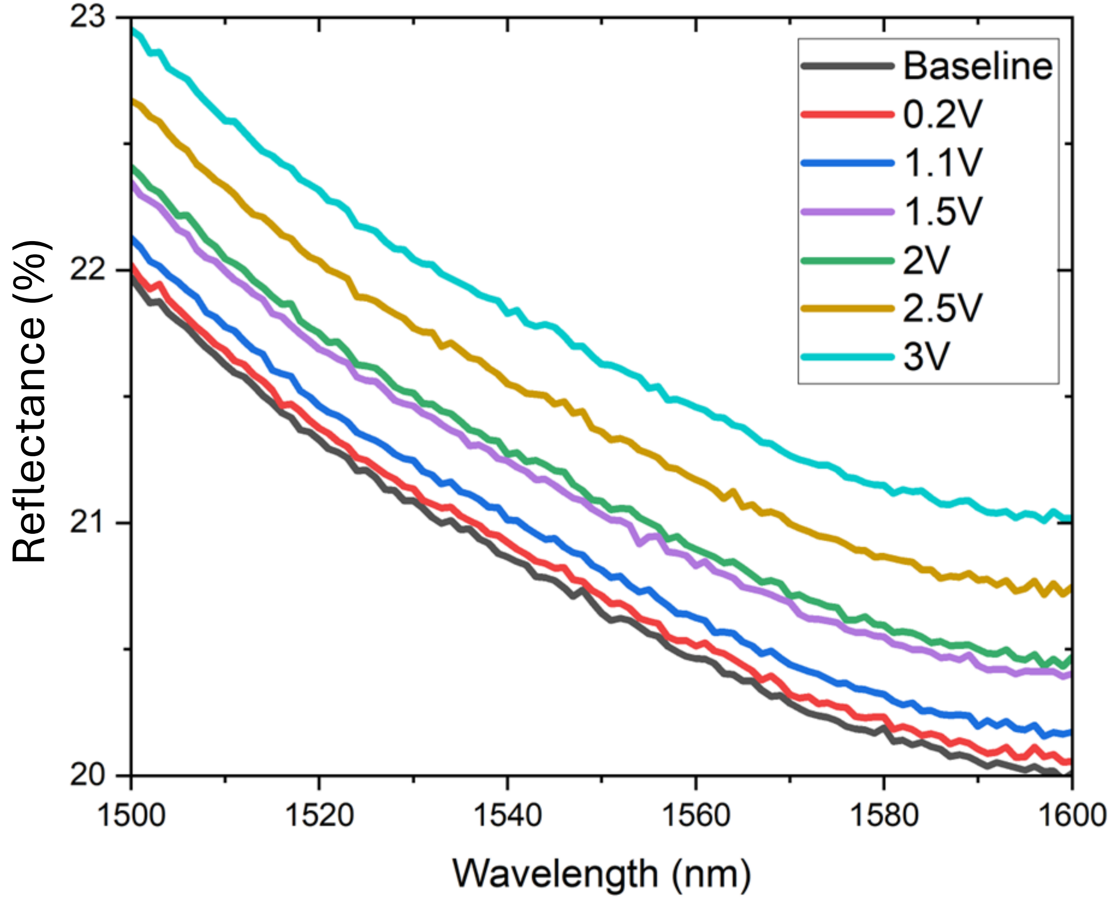




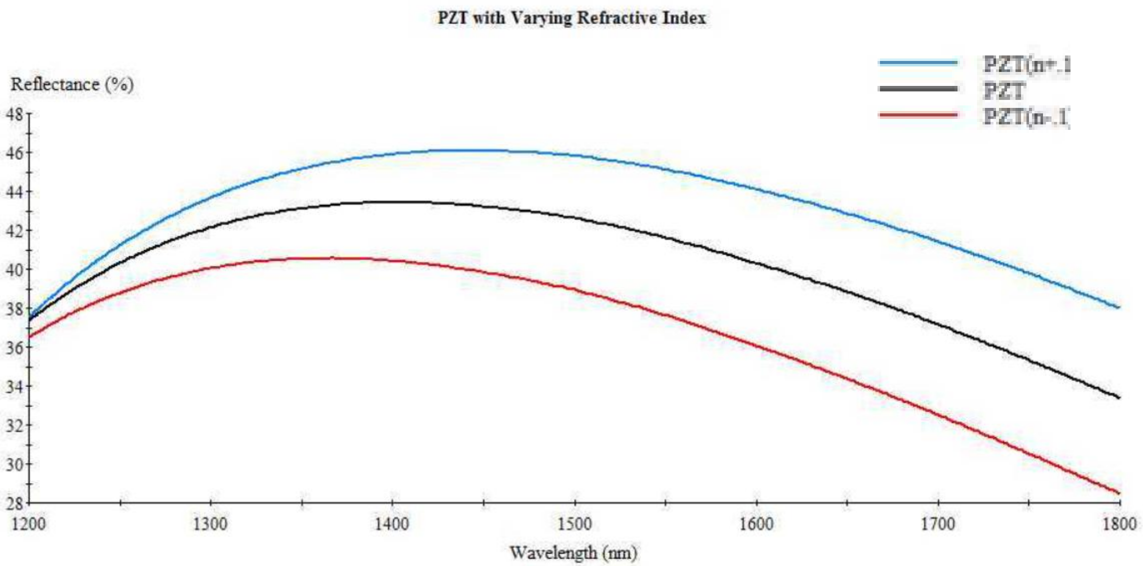
PML Validation Experiment

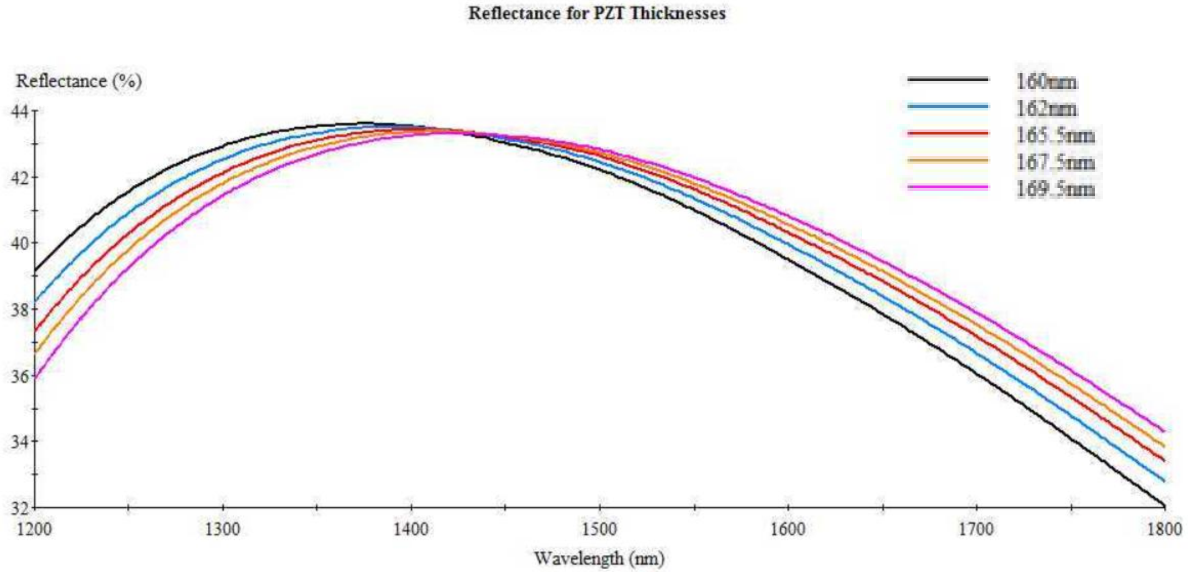
Validation Experiment Results

- Maximum voltage applied 3 V
  - Small iterations between each measurement
  - 1.0 % change in reflectance between baseline and 3 V case
  - Maximum voltage is limited by current through the sample
    - Reaching current densities of around 40 $\mathrm{mA/mm^2}$
- Currently not annealed nor is a heated platen used during the sputtering process
- Exploring other metal contact stacks



PML Validation Experiment





Macleod Simulations

- Refractive index change of ± 0.1 results in ~5% reflectance change
- Thickness change of ± 5 nm results in ~1% reflectance change

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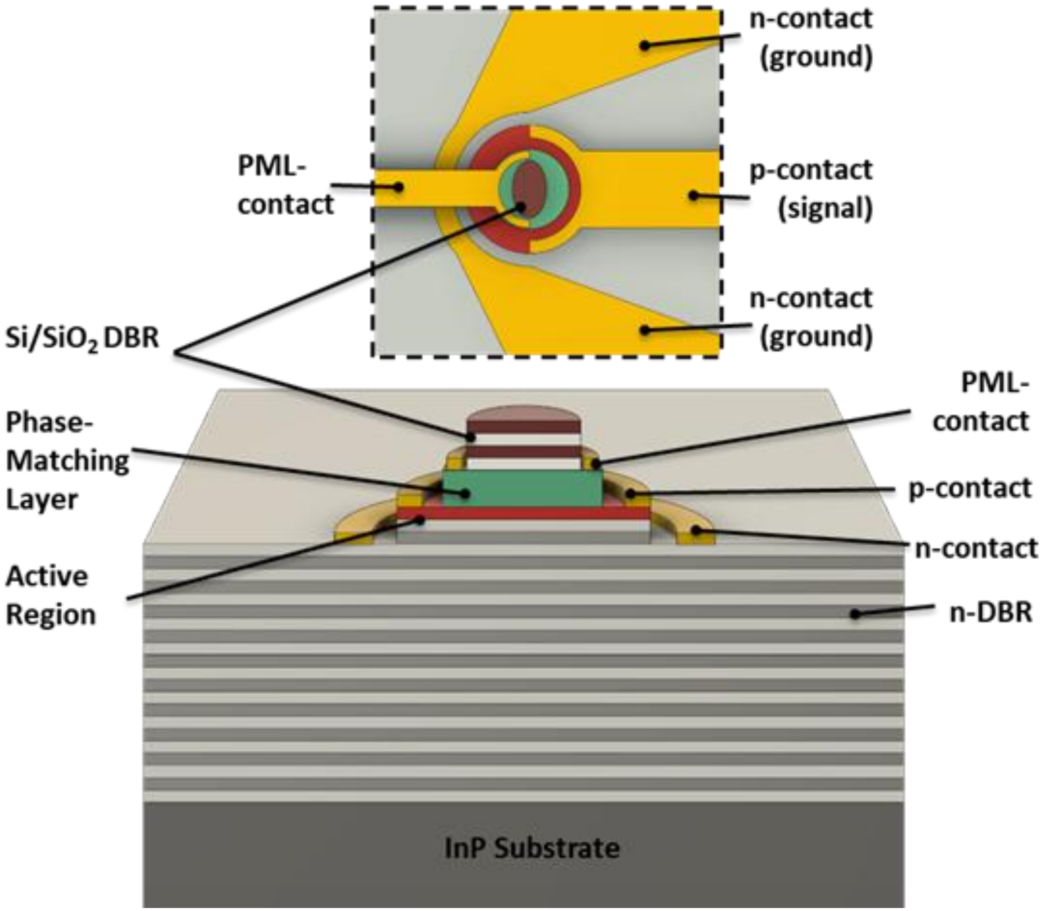


Long-wavelength VCSEL structure with dielectric top DBR and phase-matching layer

Block-Gift Grant Tasks & Milestones

Tasks in Year 1	Tasks in Year 2	Tasks in Year 3
✓ 1.1: Design of 1550 nm VCSEL epitaxial structure ✓ 1.2: TMM Simulations of full epitaxial structure including bottom DBR, PML, and dielectric top DBR ✓ 1.3: Optimization of Phase-Matching Layer Structure ○ 1.4: Development of bonding process for PML material and epitaxial material ✓ 1.5: Development of p-DBR deposition techniques ○ 1.6: Benchmarking of electro-optic performance for VCSEL epitaxial structure via electroluminescence measurements	○ 2.1: Deposition of dielectric DBR atop PML bonded to epitaxial material ○ 2.2: Mask design and layout of 1550 nm VCSELs ○ 2.3: Process flow and fabrication of 1550 nm VCSELs ○ 2.4: Benchmark of 1550 nm VCSELs for output power and spectral performance	○ 3.1: TMM simulations of single-mode, single-polarization VCSELs design ○ 3.2: Mask design and layout of single-mode, single-polarization VCSELs ○ 3.3: Process flow and fabrication of single-mode, single-polarization 1550 nm VCSELs ○ 3.4: Characterization of VCSELs for single-mode, single-polarization performance ○ 3.5: Characterization of modulation response in 1550 nm VCSELs

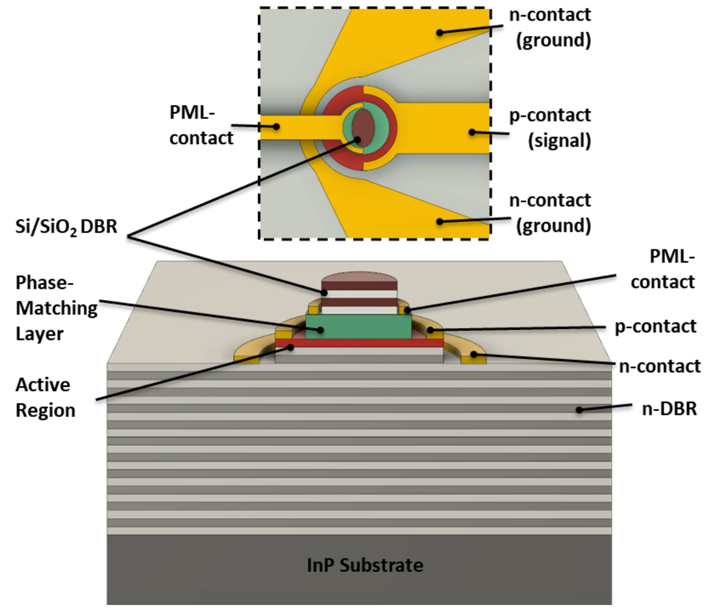
Long-Wavelength VCSELs-Conclusion

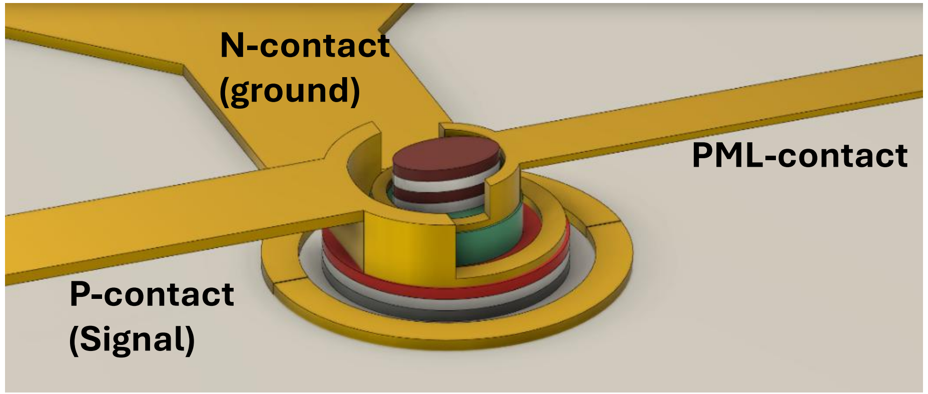
Completed Work

- Designed and simulated several epitaxial structures for 1550 nm operation
- Identified, simulated, and demonstrated viability of PZT thin film PML

Next Steps

- Optimize PZT phase matching layer
  - Develop annealing process for the PZT film
  - Identify PML contact metal stack-up
- Get the epitaxial structure for the active region grown
- Benchmark electro-optic performance of VCSEL epitaxial structure via electroluminescence measurements





Acknowledgements

The authors are grateful for the support from the Coherent/II-VI Foundation.

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Back-Up Slides

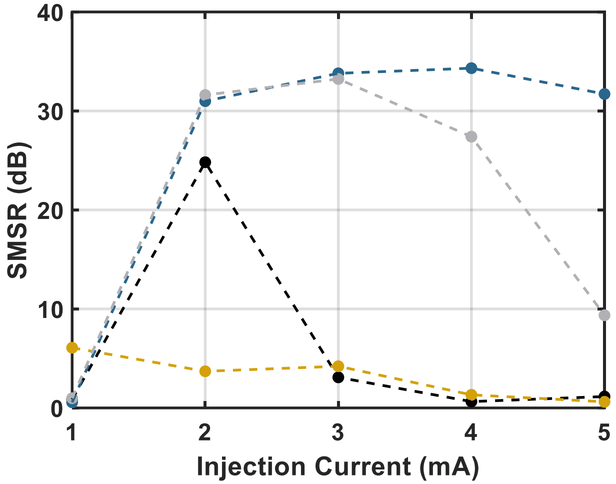
Enhanced APC VCSEL Performance

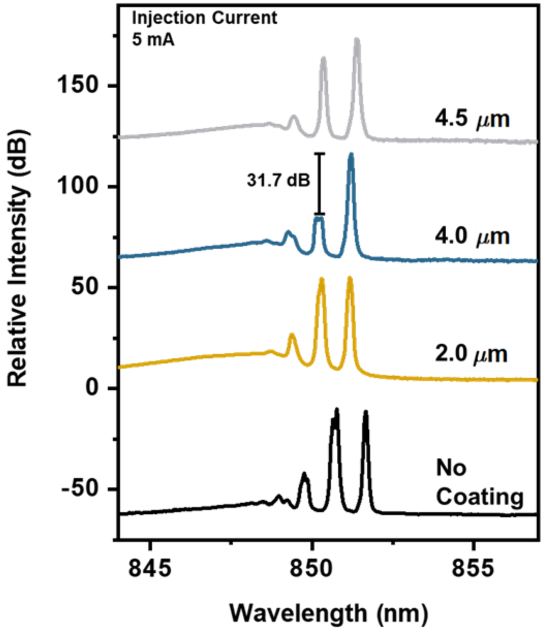
Anti-Phase VCSEL Geometry

- Mesa Size: **26 µm**
- Oxide Aperture: **4 µm**
- Anti-Phase Coating Aperture: **4 µm**

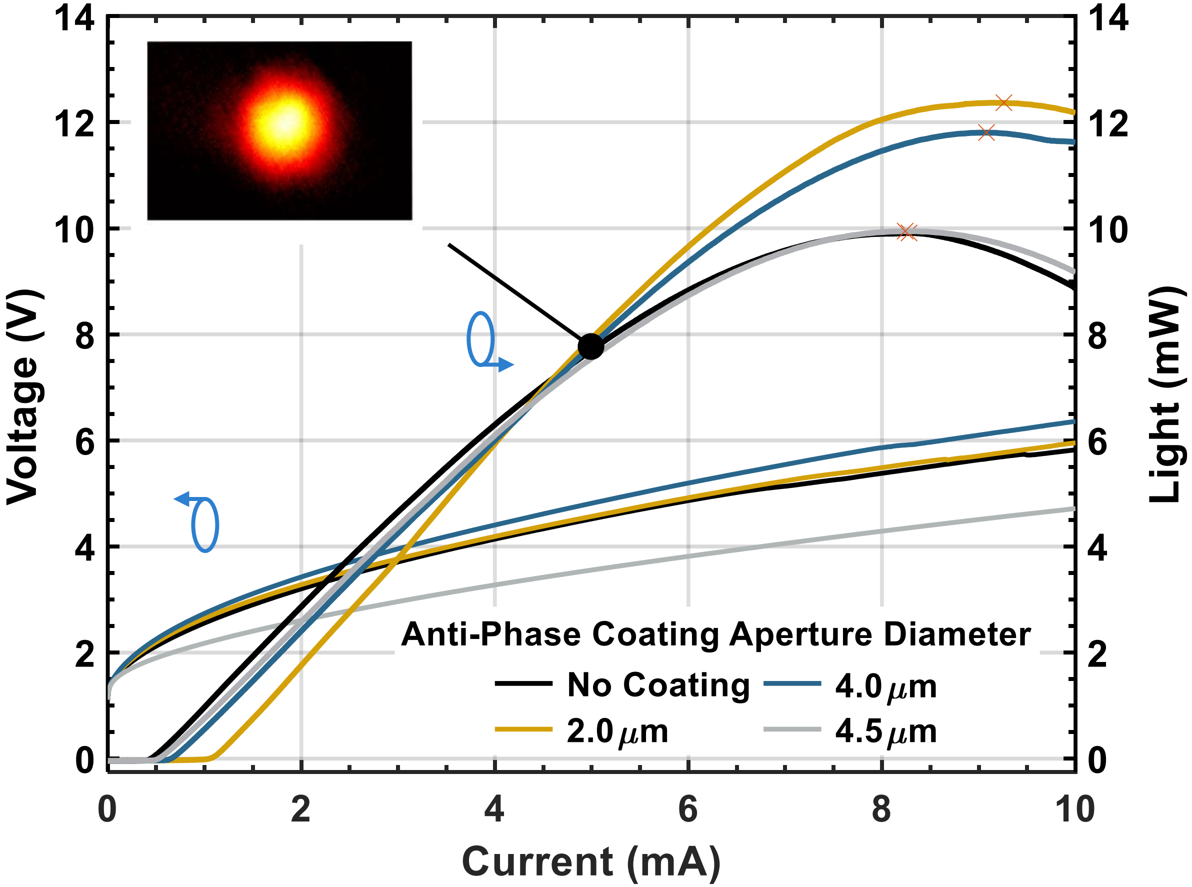
Anti-Phase VCSEL Performance

- **I_{th}= 0.62 mA**
- Peak Single-Mode Output Power: **7.48 mW**
- Thermal Rollover Current: **9.08 mA**



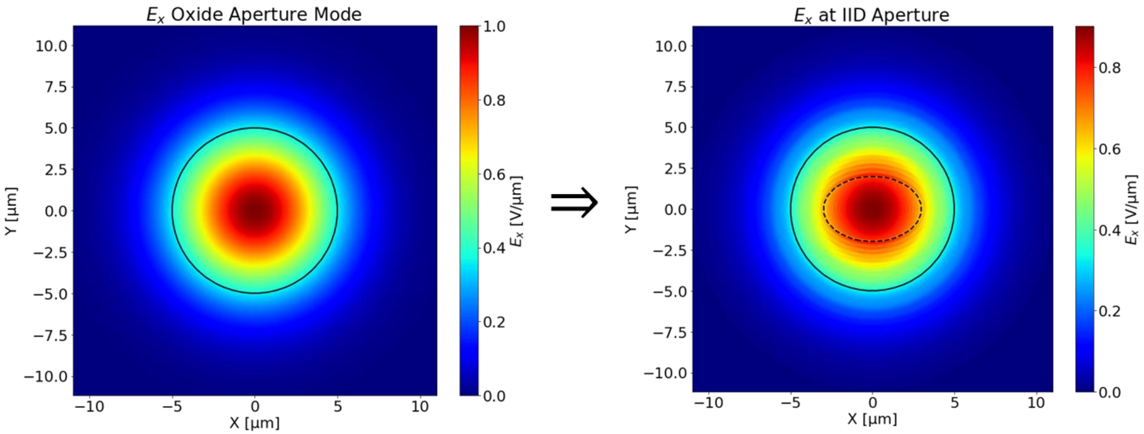


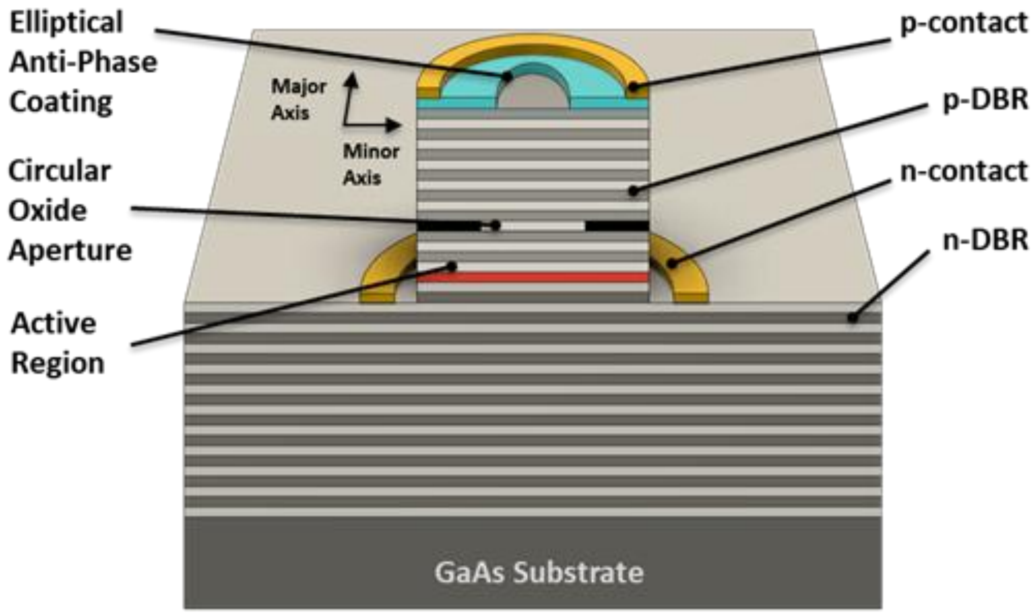
LIV-Curve of 4 µm OA VCSEL with APC



Single-Polarization VCSELs using Elliptical Apertures

- Retain circular oxide aperture to maintain cylindrical symmetry of optical transverse modes
- By introducing an **elliptical anti-phase coating aperture**, an asymmetric threshold gain (dichroism) is imparted into cavity
- With sufficient dichroism, the undesired polarization state can be partially or permanently suppressed, leading to **single-polarization operation**
- Despite operating in a single polarization state, multiple transverse modes can still be present





Single-Polarization VCSELs using Elliptical Apertures

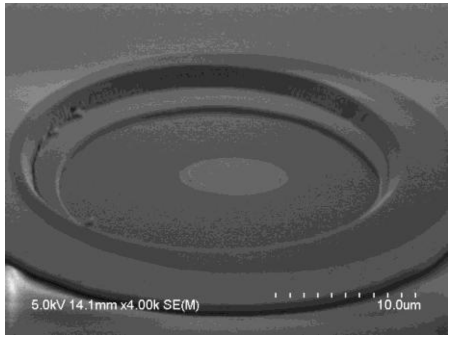
Critical Dimension Limits

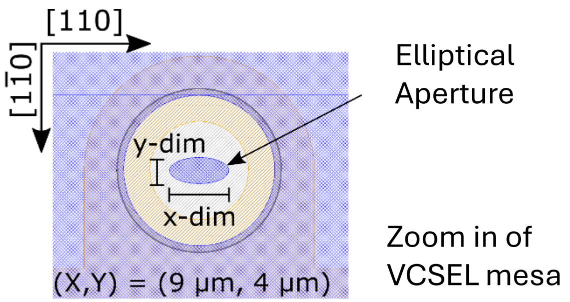
1. Circular aperture does not adequately suppress polarization states
2. Too eccentric of aperture suppresses undesired polarization state <u>but</u> impinges onto transverse modes, limiting OPSR
3. Too small of aperture suppresses all transverse modes <u>including</u> fundamental mode, limiting output power

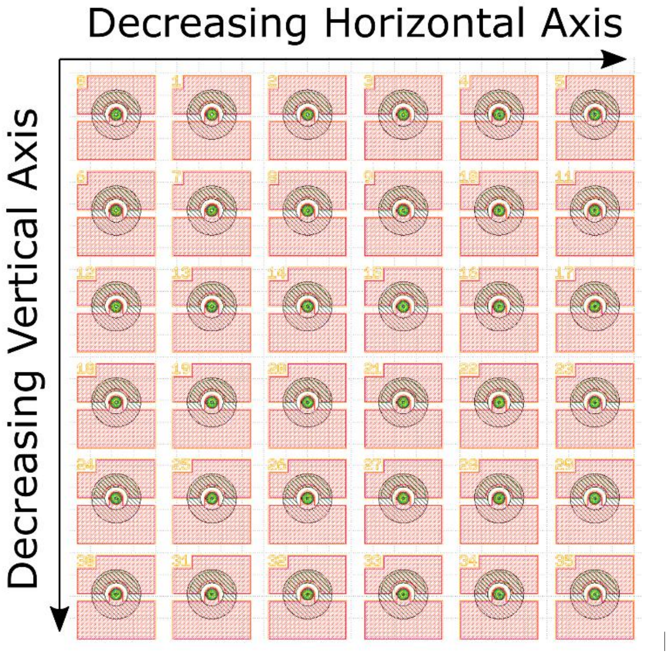
Goal

Fairly large (~active region size), slightly elliptical aperture balances undesired polarization state suppression, higher-order mode suppression, and maximizing output power

- Discovered in previous experiment [IID VCSEL paper]







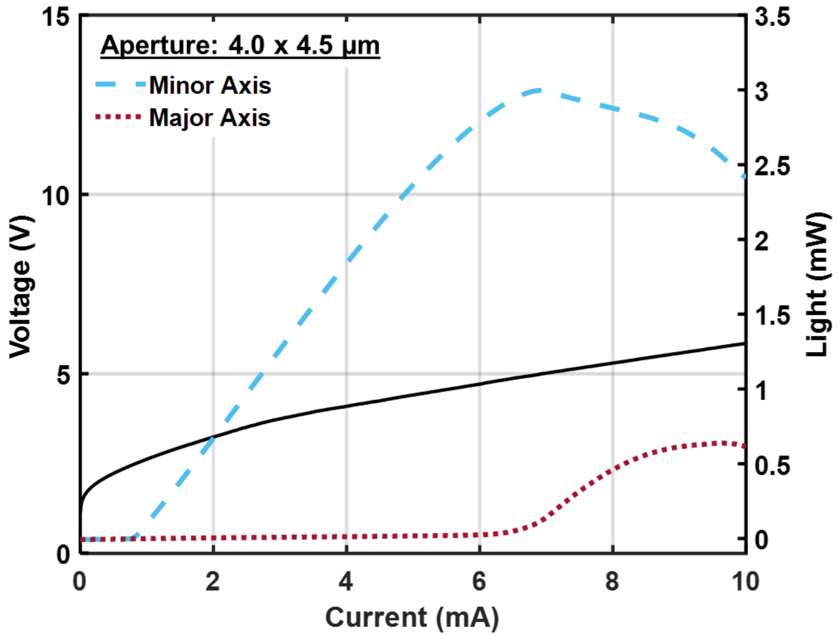
Single-Section Layout

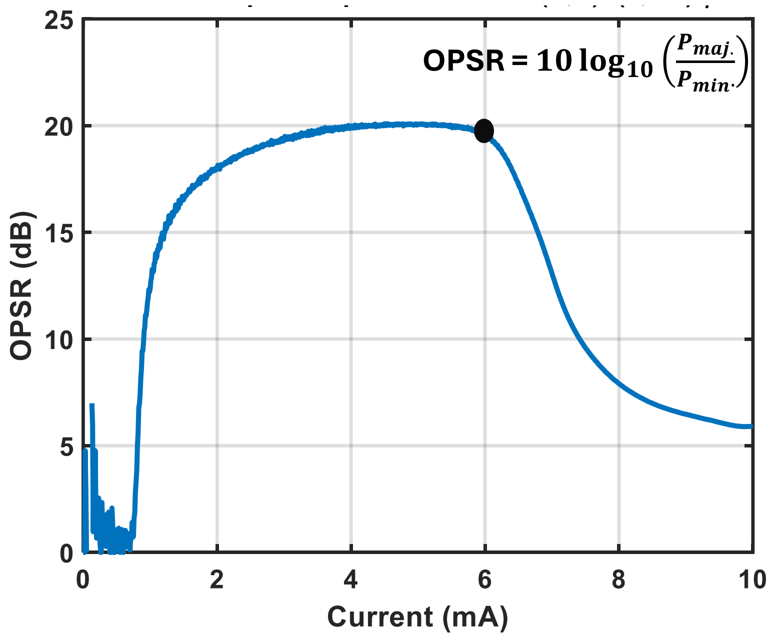
Elliptical Aperture Dimensions (X,Y) [µm]

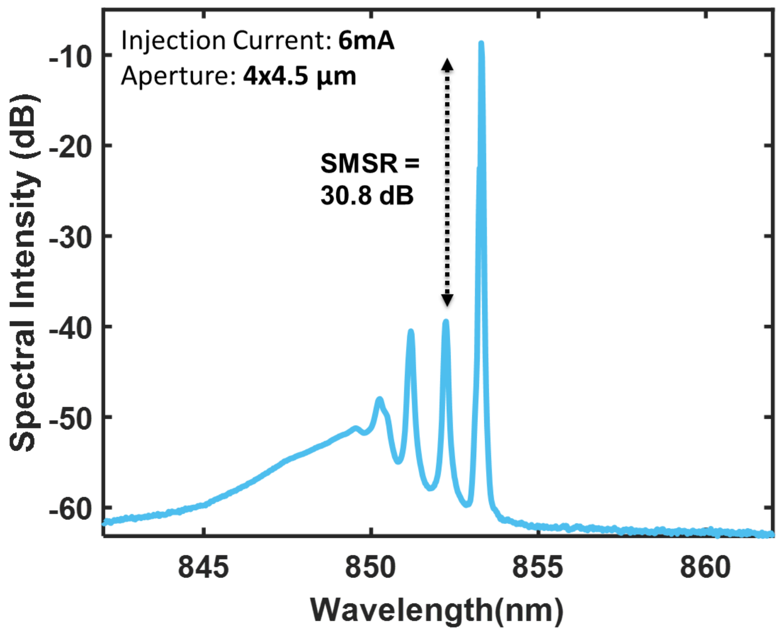
(9,9)	…	(7,9)	…	…	(4,9)
…	(8,8)				
(9,7)		(7,7)			
…			…		
…				…	
(9,4)					(4,4)

Elliptical Aperture Sizes (X,Y) [µm]

Single-Mode, Single-Polarization Operation







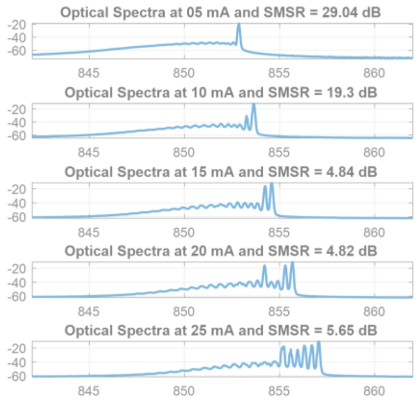
- Slightly elliptical anti-phase coating aperture suppresses undesired polarization state without undesired encroachment onto fundamental transverse mode, resulting in 3 mW of output power
- OPSR of 20 dB measured at 6mA, achieving **single-polarization operation**
- SMSR of 30.8 dB measured, indicating simultaneous **single-mode operation** with **2.79 mW** of output power

Disordered VCSELs with Anti-Phase Coating

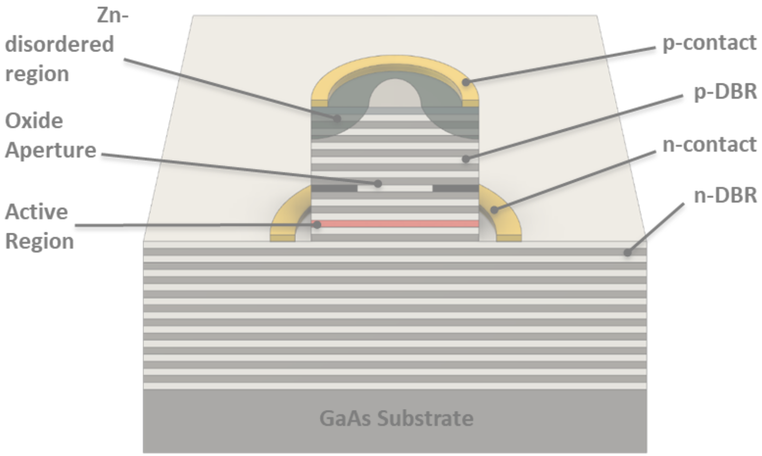
<u>Goal</u>

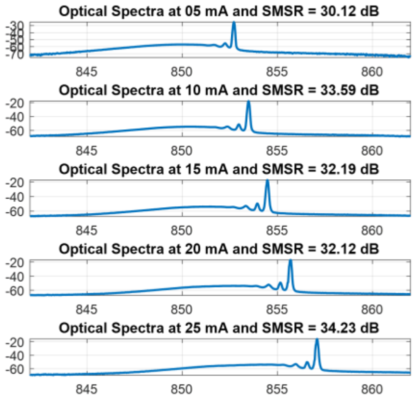
Deposit anti-phase coating onto <u>multi-mode disorder-defined VCSELs</u> to suppress higher-order modes and <u>achieve single-mode operation</u>

- Previously fabricated VCSELs with disorder-defined apertures operate in multiple higher-order modes due to large disorder-defined aperture
- Deposit anti-phase coating with patterned aperture, suppressing higher-order modes and achieving single-mode operation
- Combination of two mode-control techniques, aim to work together should one experience issues

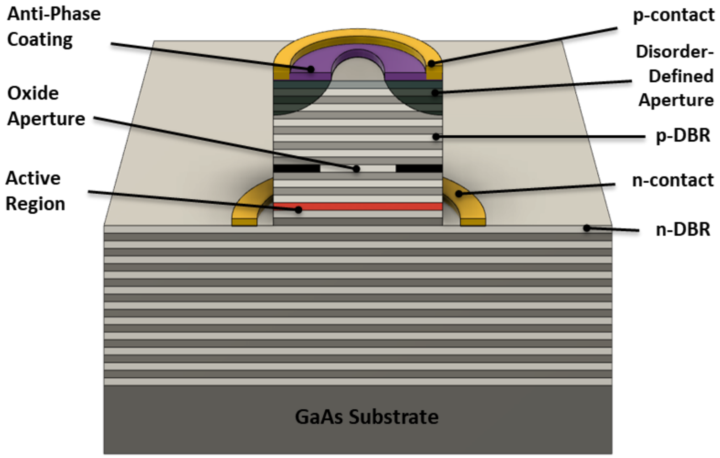


Before



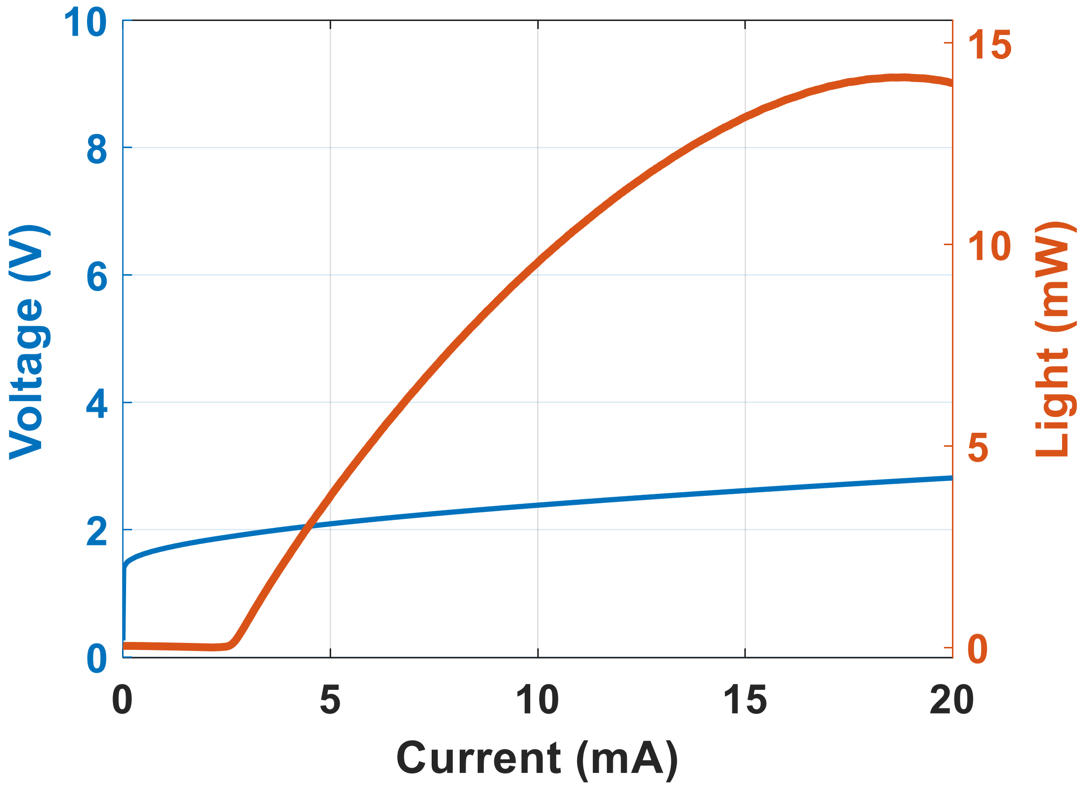


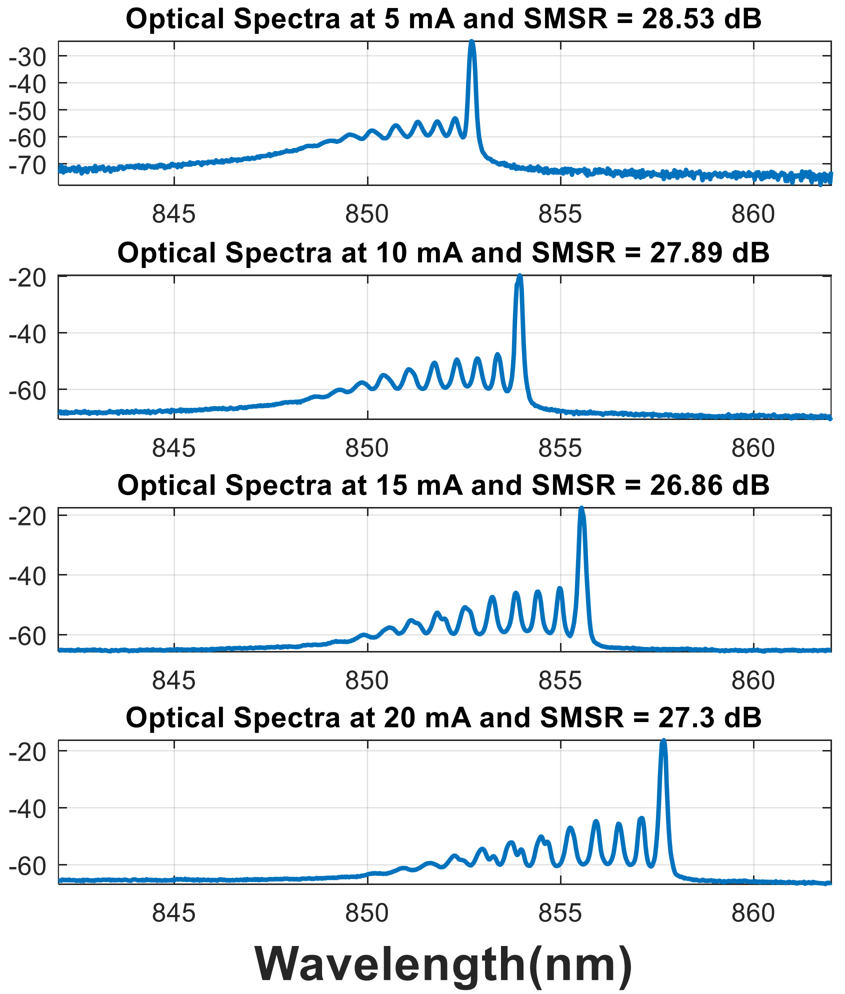
After



Disordered VCSELs without Anti-Phase Coating

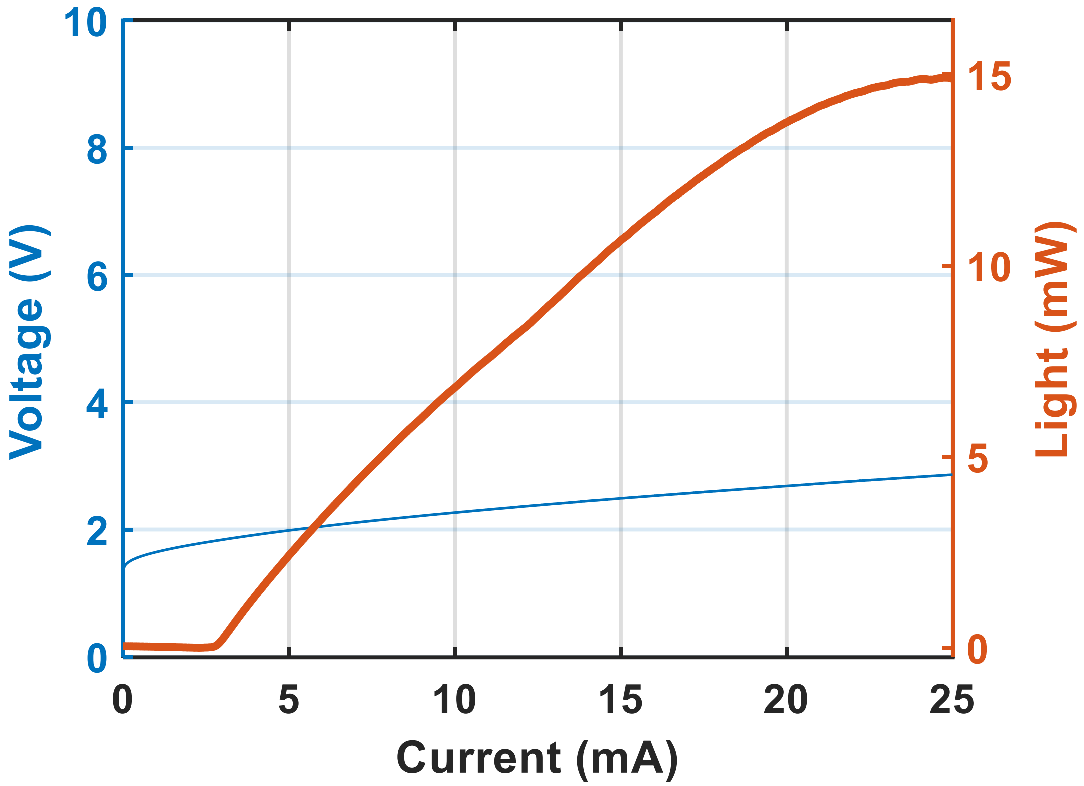
Oxide Aperture	IID Aperture	APC Aperture	Peak Single Mode Power
9 µm	4.15 µm	N/A	N/A

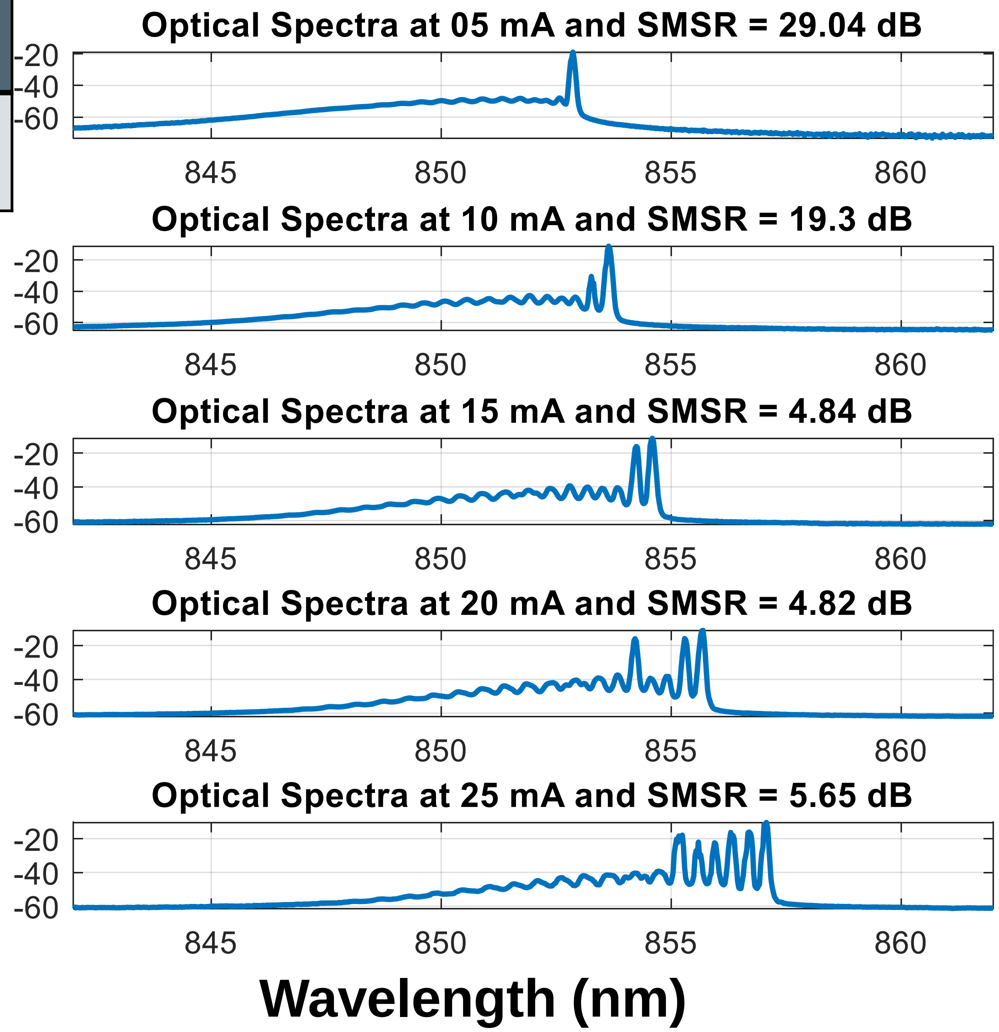




Disordered VCSELs without Anti-Phase Coating

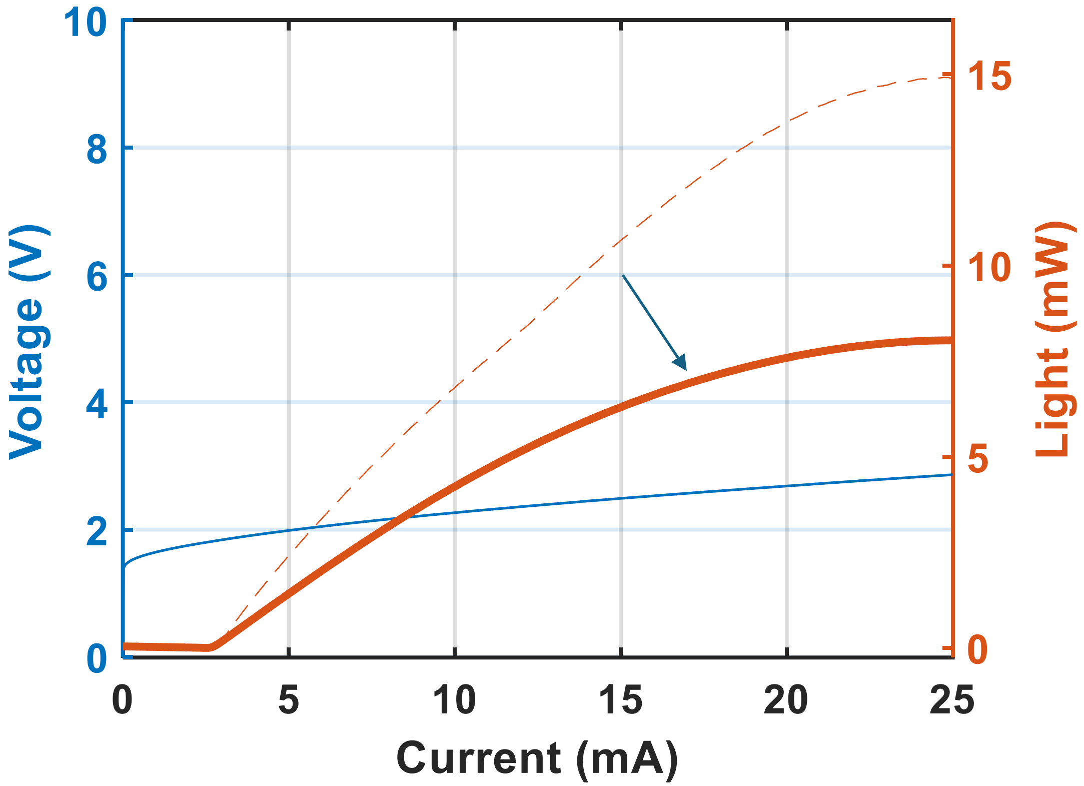
Oxide Aperture	IID Aperture	APC Aperture	Peak Single Mode Power
<u>13 µm</u>	<u>6.1 µm</u>	N/A	N/A

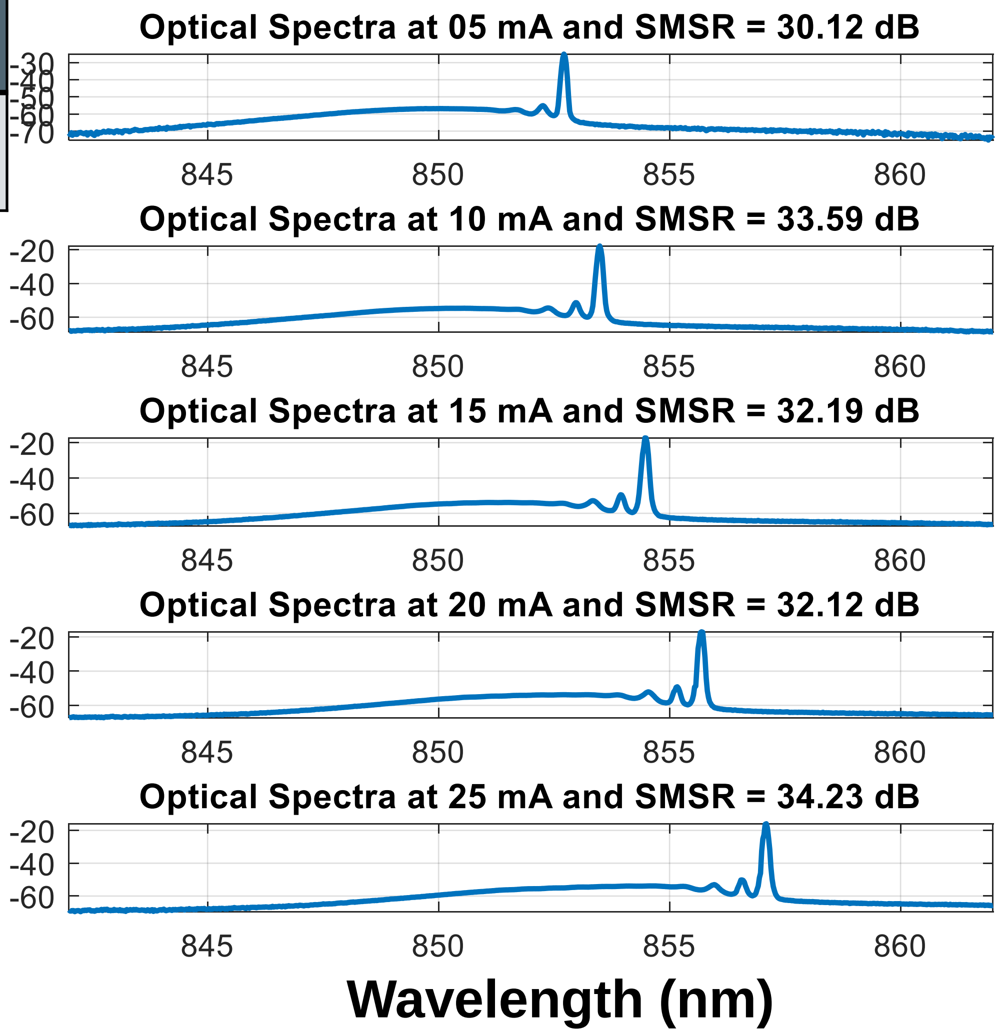




Disordered VCSELs with Anti-Phase Coating

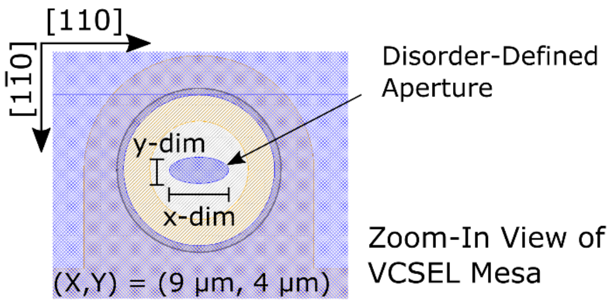
Oxide Aperture	IID Aperture	APC Aperture	Peak Single Mode Power
13 µm	6.1 µm	3.5 µm	8.1 mW





Disorder-Defined Aperture VCSEL 2D-Arrays

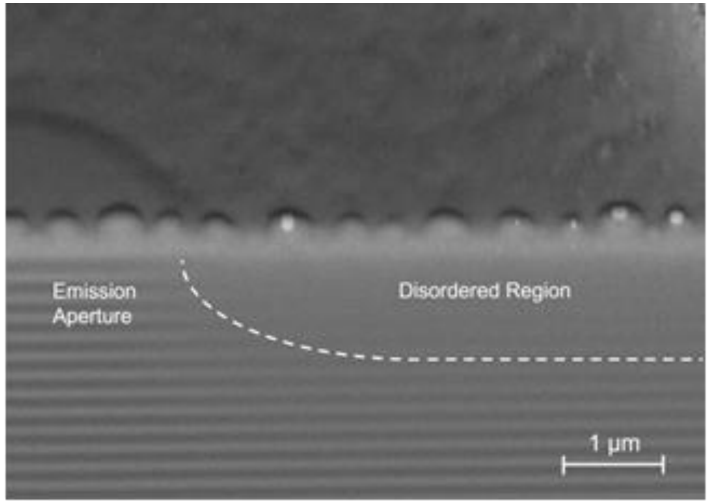
- Motivation: High-power single-mode, single-polarization arrays for 3D-sensing and LiDAR
- 2D-arrays designed with various pitches (15-30 um in 5 μm steps), active region and aperture sizes, and number of devices (5 and 9)
- Incoherent arrays due to large pitch size and lack of evanescent light coupling between devices

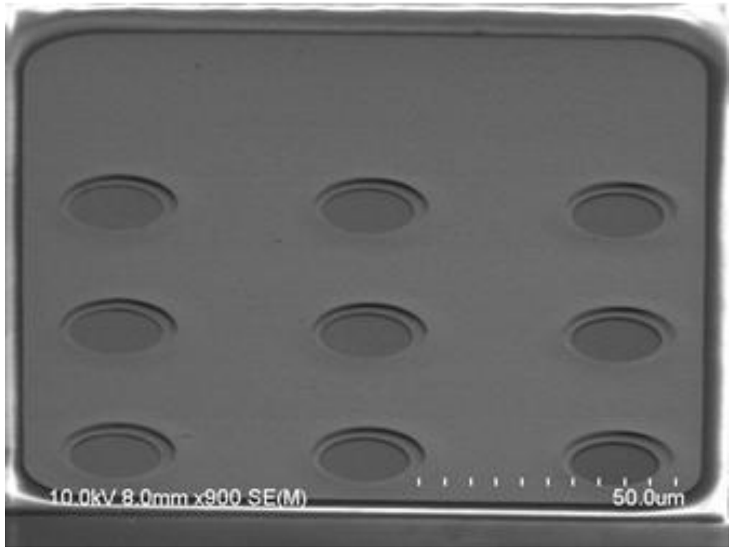


Disorder-Defined Aperture Elliptical (X,Y) Dimensions [μm]

(9,9)	...	(7,9)	...	...	(4,9)
...	(8,8)				
(9,7)		(7,7)			
...			...		
...				...	
(9,4)					(4,4)

Disorder-Defined Aperture Sizes

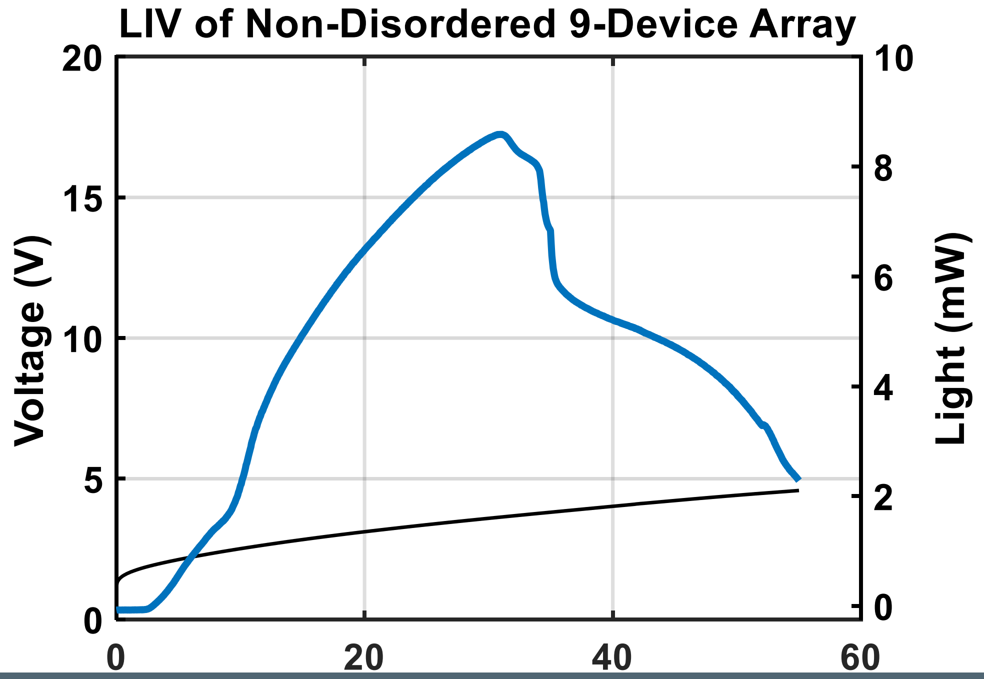


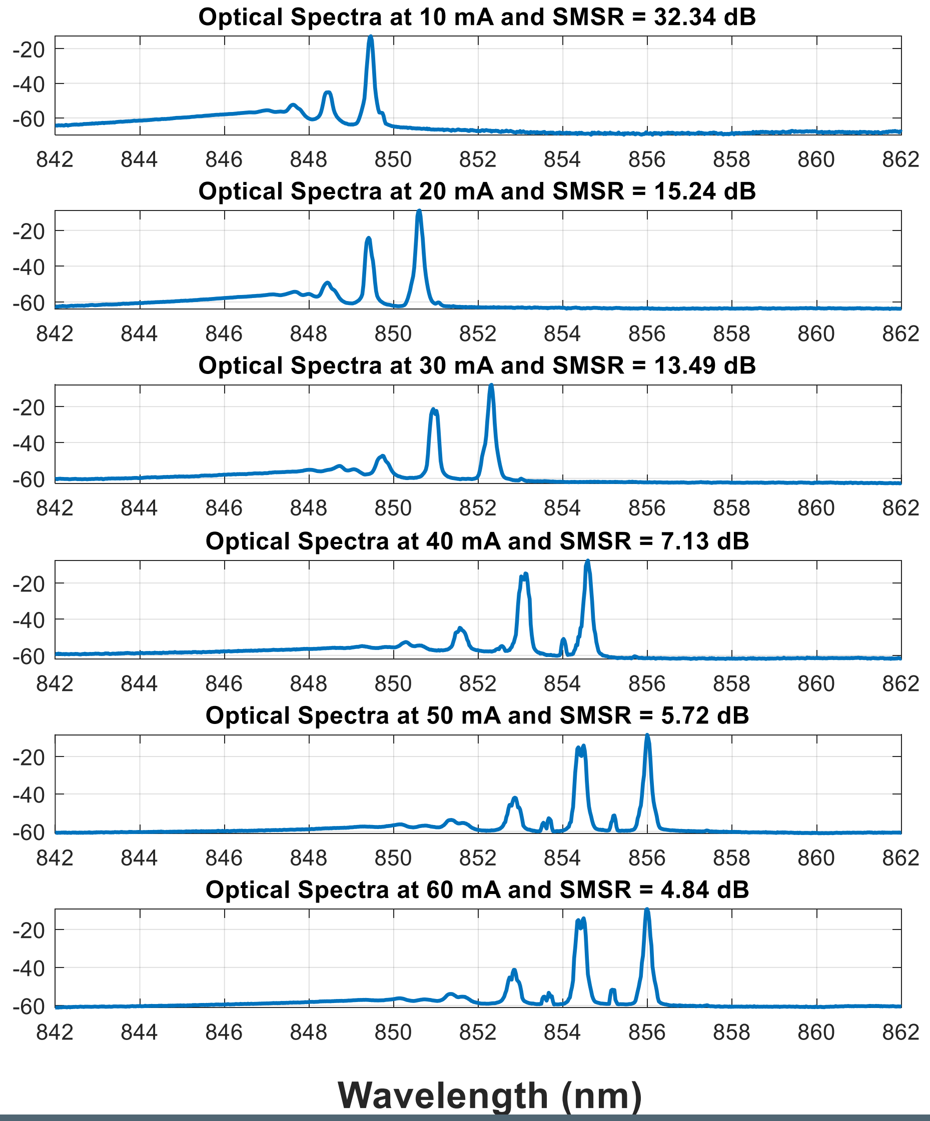


Nondisordered 9-VCSEL Array- 25 µm pitch

- Active region: 11 µm
- Disordered Aperture: none

- Peak Single-Mode Output Power (measured with integrating sphere): **N/A**

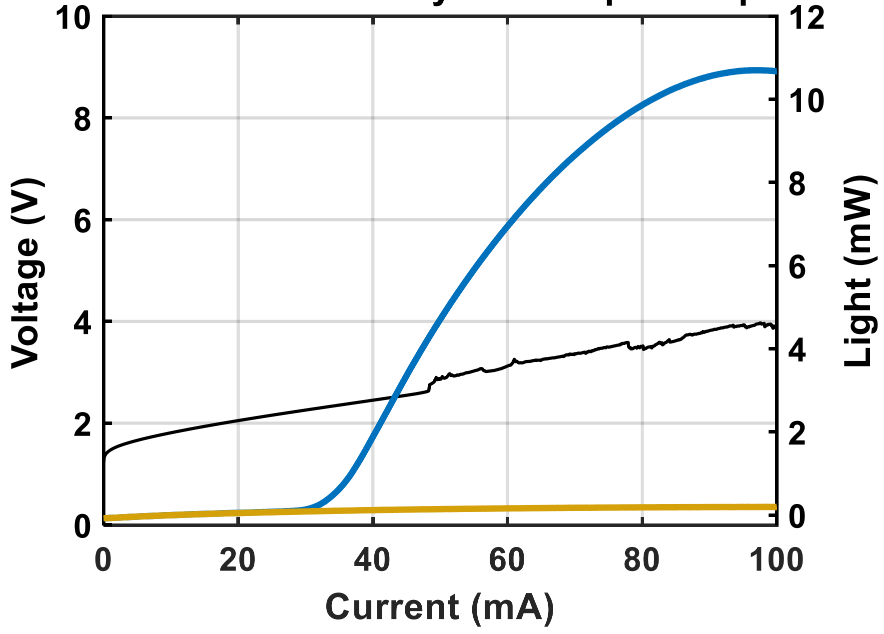


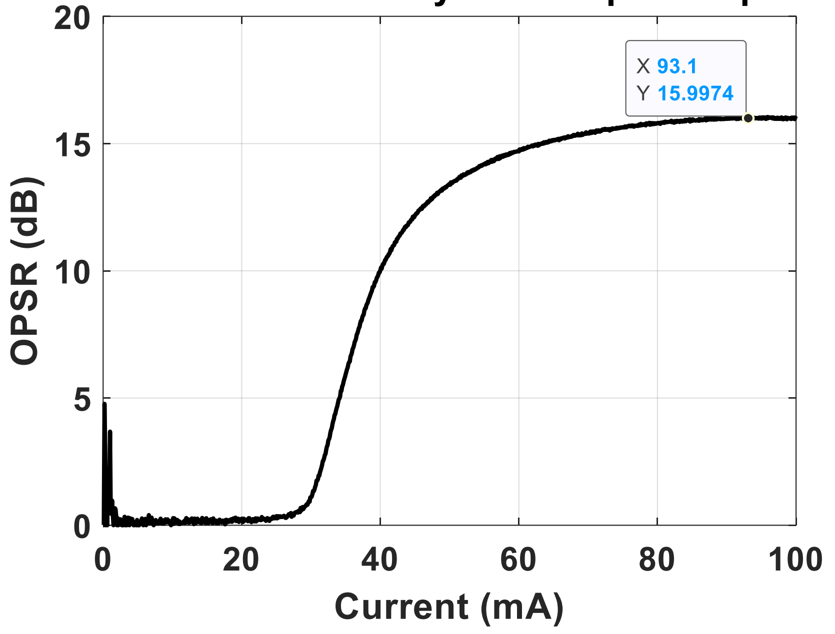


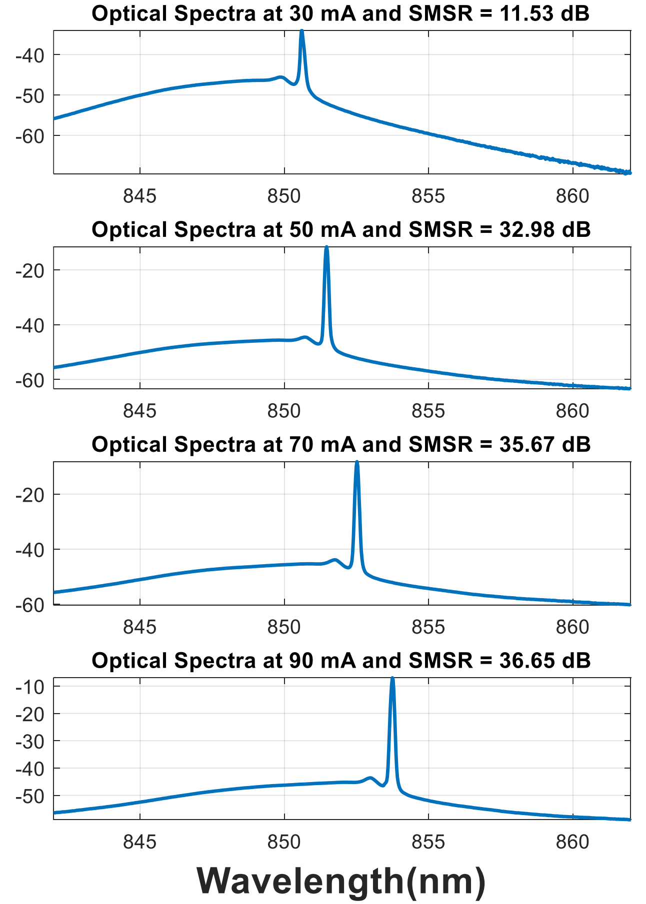
Disorder-Defined Aperture VCSEL 2D-Arrays-Elliptical Aperture

- Active region: 11 μm
- Disordered Aperture: 4 x 5 μm

- Peak Single-Mode Output Power (measured with integrating sphere): **10.7 mW**







Disordered 9-VCSEL Array - 30 µm pitch - Circular Apertures

- Active Region: 11 µm
- Disordered Aperture: 5 µm

- Peak Single-Mode Output Power: **16.22 mW**
- Single-Mode Output Power Per Device: **1.8 mW**
- Peak OPSR: **19. 1dB**
- Threshold Current: **20.6 mA**